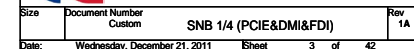


Table of Contents

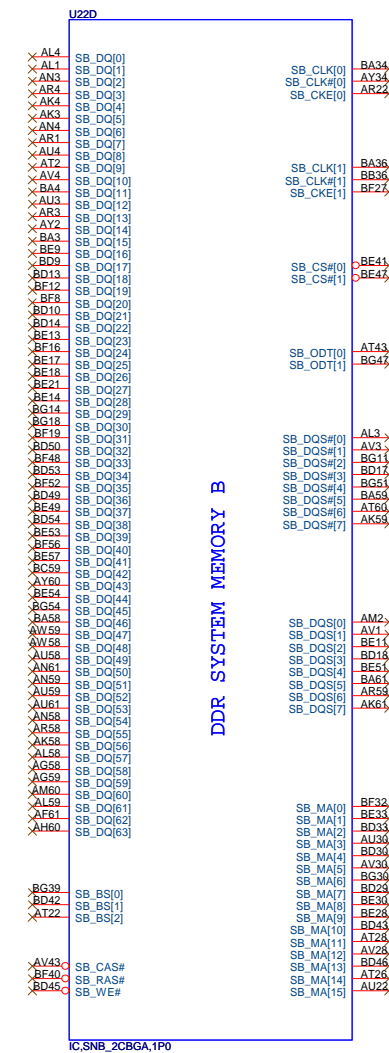
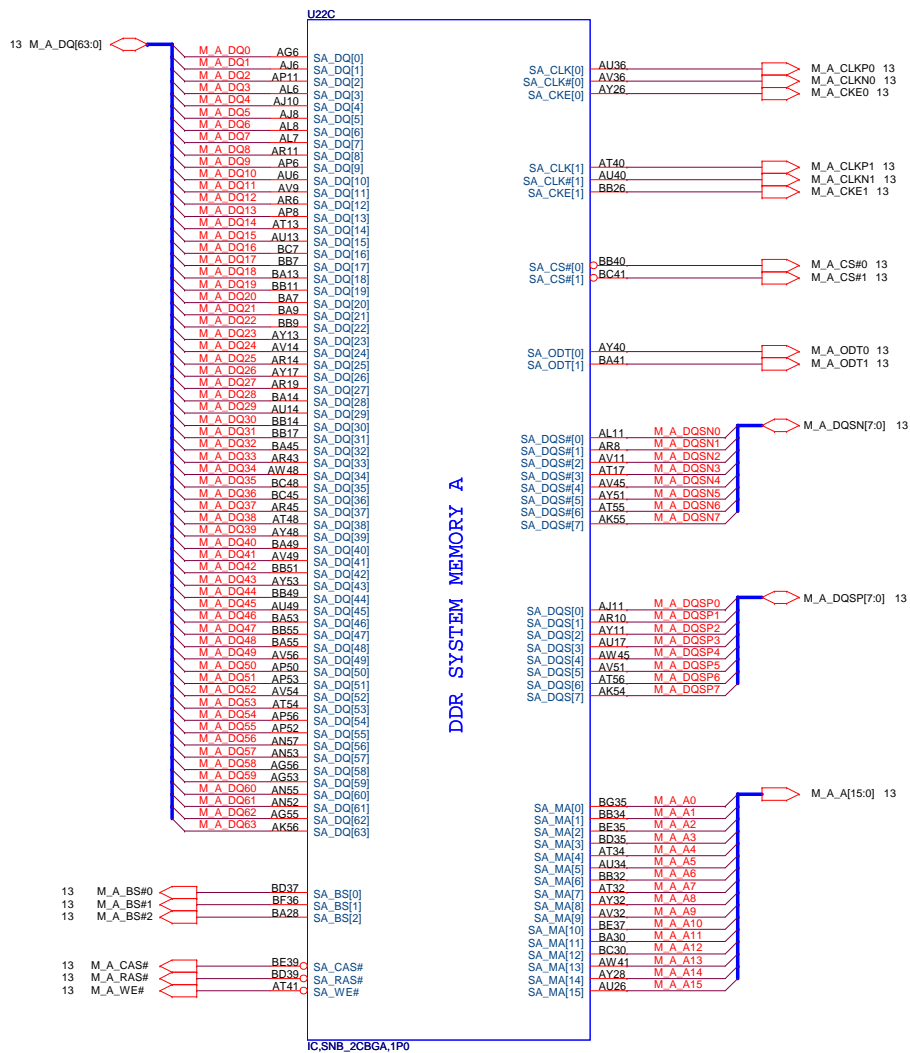
PAGE	DESCRIPTION
01	LOCK DIAGRAM(UMA)
02	FRONT PAGE
03-06	Sandy Bridge
07-12	Cougar Point-PCH
13	DDRIII SO-DIMM
15	PS8622 LVDS converter
16	LCD/CAMERA
17	HDMI CONN
18	AUDIO (CX20671-21Z, SPK)
19	LAN[RTL8105E]
20	SATA
21	Card Reader-AU6435B52-GDL
22	USB2.0 X2/USB3.0 X2
23	MINI Card (SSD)
24	WLAN/BT
25	KB/TP/LID/AUDIO USB Conn
26	Blank
27	FAN/Thermal
28	KBC IT8518/19
29	SW/LED
30	Screw Hole/EMI/ESD
31	Power Block Diagram
32	3V/5V (TPS51123ARGERR)
33	Discharge
34	CHARGER (BQ24725)
35	DDR3/0.75V (TPS51216)
36	+1.05V(RT8240B)
37	VCCSA (RT8241A)
38	1.8V(TPS54318)
39	CPU(ISL95831)JIMVP1+1
40	Power On Sequence
41	EC RECORD DV
42	Power EC RECORD DV
43	
44	
45	
46	
47	

Power States

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	10V~+20V	16, 32, 34, 35, 36, 37, 39	MAIN POWER		S0~S5
+3V_RTC	+3.0V~+3.3V	7, 8, 11, 28	RTC		S0~S5
3VPCU	+3.3V	8, 16, 19, 25, 28, 29, 32, 33, 34, 38	IT8518/19 POWER	3V5V_EN	S0~S5
5VPCU	+5V	16, 32, 33, 35, 36, 37, 38, 39	DC/DC POWER IC SOURCE	3V5V_EN	S0~S5
15V	15V	16, 32, 33, 35	LARGE POWER	3V5V_EN	S0~S5
LANVCC	+3.3V	19, 33	LAN POWER	LAN_ON	
5V_S5	+5V	11, 22, 33	PCH SUS POWER	S5_ON	S0~S3
3V_S5	+3.3V	3, 7, 8, 9, 10, 11, 24, 33	Sys Management, PCH Resume Well, USB, WLAN, WiMAX POWER	S5_ON	S0~S3
5VSUS	+5V		SLP_S4# CTRLD POWER	SUSON	S0~S3
3VSUS	+3.3V		SLP_S4# CTRLD POWER	SUSON	S0~S3
1.5V_SUS	+1.5V	3, 11, 13, 33, 35	DDR3 SODIMM POWER	SUSON	S0~S3
+0.75V_DDR_VTT	+0.75V	7, 11, 16, 17, 18, 20, 27, 33, 34	DDR3 SODIMM REFERENCE POWER	MAINON	S0
+5V	+5V	16, 32, 34, 35, 36, 37, 39	SLP_S3# CTRLD POWER	MAINON	S0
+3V	+3.3V	3, 7, 8, 9, 10, 11, 13, 15, 16, 17, 18, 19, 20, 21, 23, 24, 25, 27, 28, 32, 33, 34, 35, 36, 37, 38, 39	SLP_S3# CTRLD POWER	MAINON	S0
+VCC_GFX		5, 39	VGA CORE POWER	MAINON	S0
VCCSA	+0.8V~+0.9V	5, 33, 37	Sandy Bridge Power	MAINON	S0
+1.8V	+1.8V	5, 8, 11, 33, 38	LVDS, NVM POWER	MAINON	S0
+1.05V	+1.05V	3, 5, 7, 8, 9, 11, 15, 33, 36	Sandy Bridge VTT POWER/PCH CORE POWER	MAINON	S0
+VCC_CORE		5, 6, 39	CPU CORE POWER	VRON	S0
+LCDVCC	+3.3V	16	LCD Power	ENVDD	S0
+3V_HDD	+3V	20	ODD Power	ODD_5V_ON	S0
+5V_HDD	+5V	20	HDD Power	MAINON#	S0
BAT-V	+10V~+17V	34	MAIN BATTERY	CHG_PBATT	S0~S5
+1.5V_CPU	+1.5V	3, 5, 35	DDR3 1.5V Rails	PS_S3CNTRL	S0



Ivy Bridge Processor (DDR3)



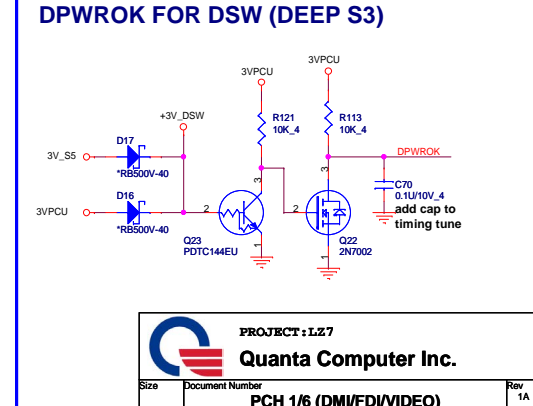
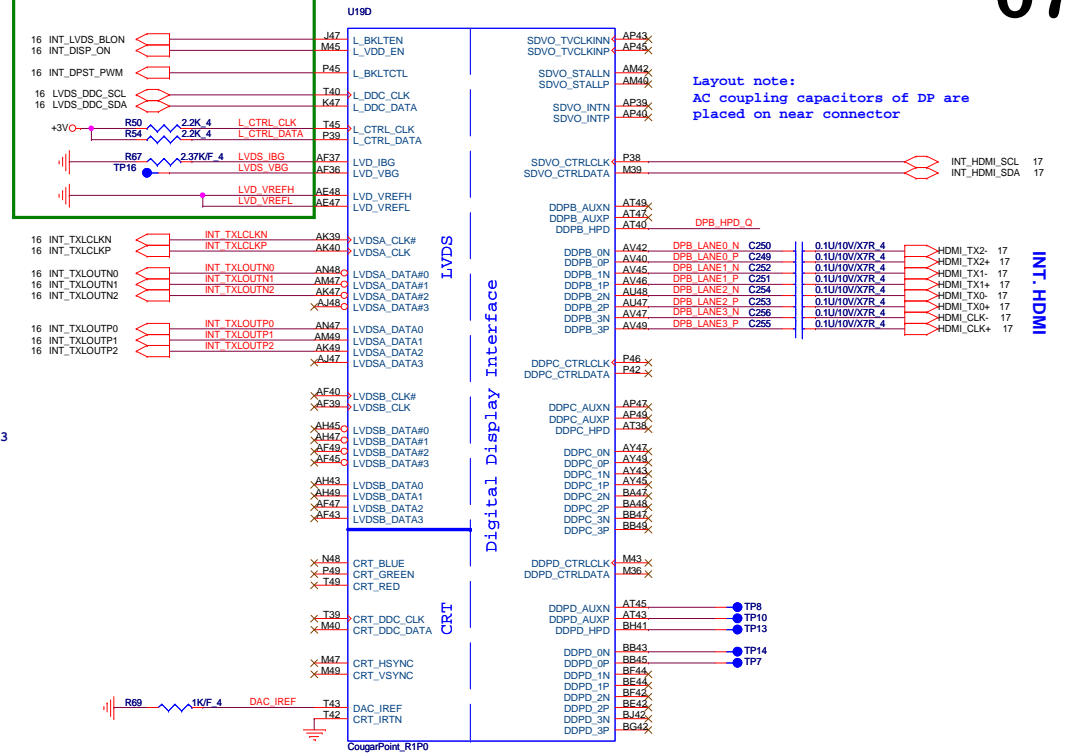
330uF locate power side

CAD Note: +VDDR_REF_CPU should have 10 mil trace width

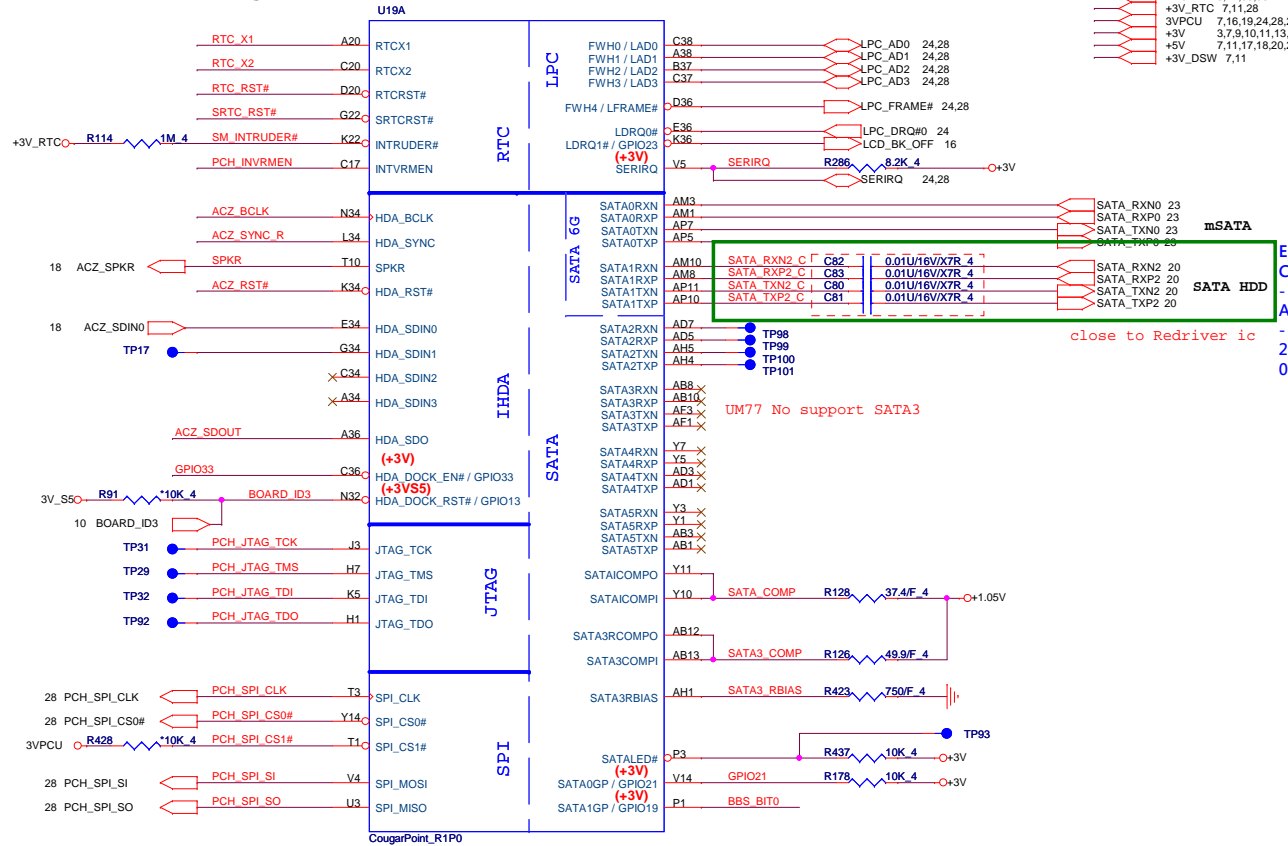
Size	Document Number Custom	SNB 3/4 (POWER)	Rev 1A
Date:	Wednesday, December 21, 2011	Sheet 5 of 42	

06





Cougar Point/Panther Point (HDA,JTAG,SATA)



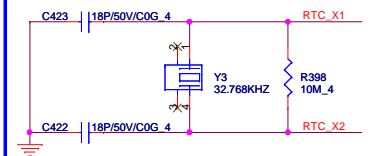
if default boot destination is SPI,
no external pull-up/-down resistors on the board are
necessary

PCH Strap Table

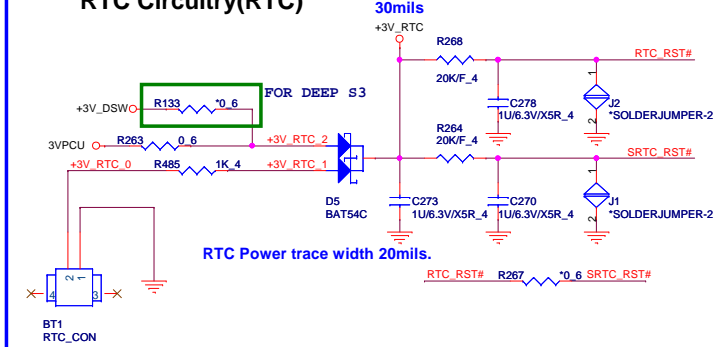
Pin Name	Strap description	Sampled	Configuration	Circuit
SPKR	Different from Calpella	No reboot mode setting	PWROK 0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	SPKR R168 *1K_4 +3V
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R26 R23 *1K_4 +3V
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	PCH_INVRMEN R399 330K_4 +3V_RTC
HDA_SDO	Flash Descriptor Security Only for Interposer	PWROK	0 = effective(Default: weak pull down) 1 = Override	ACZ_SDOUT R87 *1K_4 3V_S5
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK		[Need external pull-down for LPC BIOS]
GPIO19	Different from Calpella	Boot BIOS Selection 0 [bit-0]	PWROK	R429 R28 *1K_4 BBS_BIT0 BBS_BIT1 9
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN
DF_TVS	DMI Termination voltage IVY:0 SANDY:1	PWROK	weak pull-down 20kohm	R416 22K_4 +1.8V R415 1K_4 3 PROC_SELECT#
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	3V_S5 R85 1K_4 ACZ_SYNC_R
GPIO15	Intel ME Crypto Transport Layer Security cipher suite		Low = Disable (Default) High = Enable	10 HOST_ALERT#1 R R432 1K_4 +3V_S5
GPIO28	Different from Calpella	On-die PLL Voltage Regulator	0 = Disable 1 = Enable (Default)	R167 *1K_4 PLL_ODVR_EN 10
DSWVREN		0: disable 1: enable		

RTC Clock 32.768KHz

08

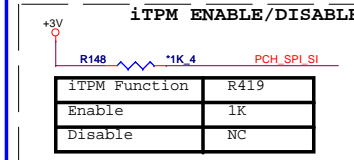


RTC Circuitry(RTC)

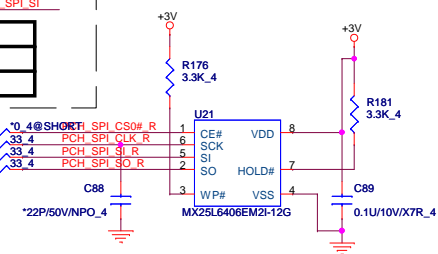


W25Q64CVSSIG: AKE3EFP0N04
MX25L6406EM2I-12G: AKE3NFP0Z00
EN25Q64-104HIP: AKE3EFN0Q00

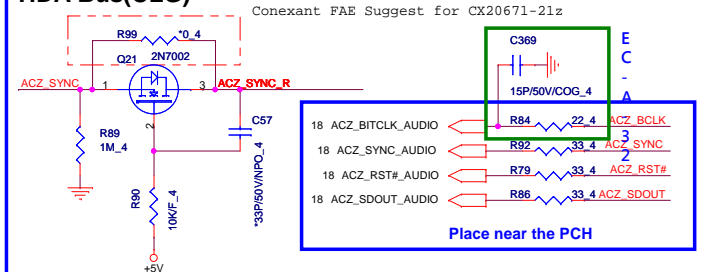
PCH Dual SPI 64Mbit (8M Byte), SPI



Socket:
P/N: DG008000031
Footprint: 91960-0084L-8P-SOCKET



HDA Bus(CLG)



PROJECT: LZ7
Quanta Computer Inc.

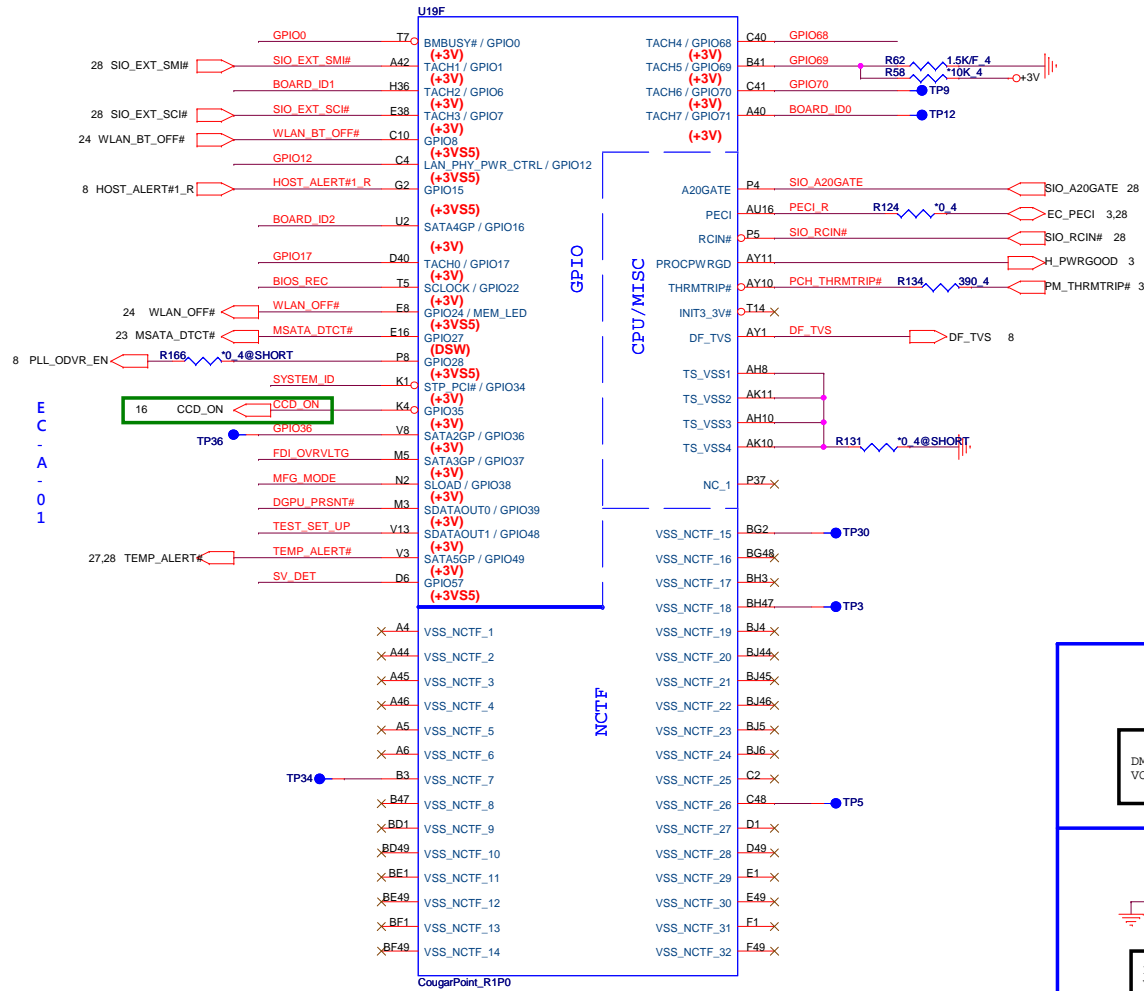
Size: Document Number
PCH 2/6 (SATA/HDA/SPI)

Date: Wednesday, December 21, 2011 Sheet 8 of 42

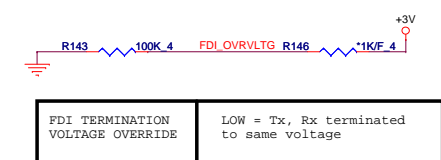
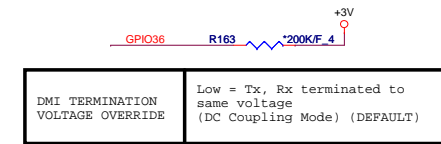
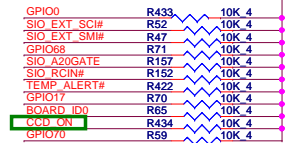
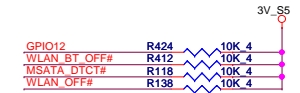
Cougar Point/Panther Point (GPIO,VSS_NCTF,RSVD)

3V_S5 3,7,8,9,11,18,24,29,33
+3V 3,7,8,9,11,13,16,17,18,19,20,21,23,24,25,27,28,32,33,34,35,36,37,38,39

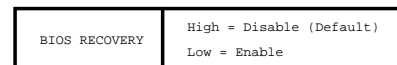
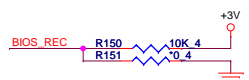
10



GPIO Pull-up/Pull-down(CLG)



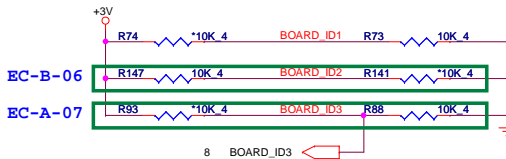
MFG-TEST



BOARD ID SETTING

Board ID For Function	ID1 GPIO6	ID2 GPIO16	ID3 GPIO13
SDV			
SIV			
SVT	0	1	0
SOVP			

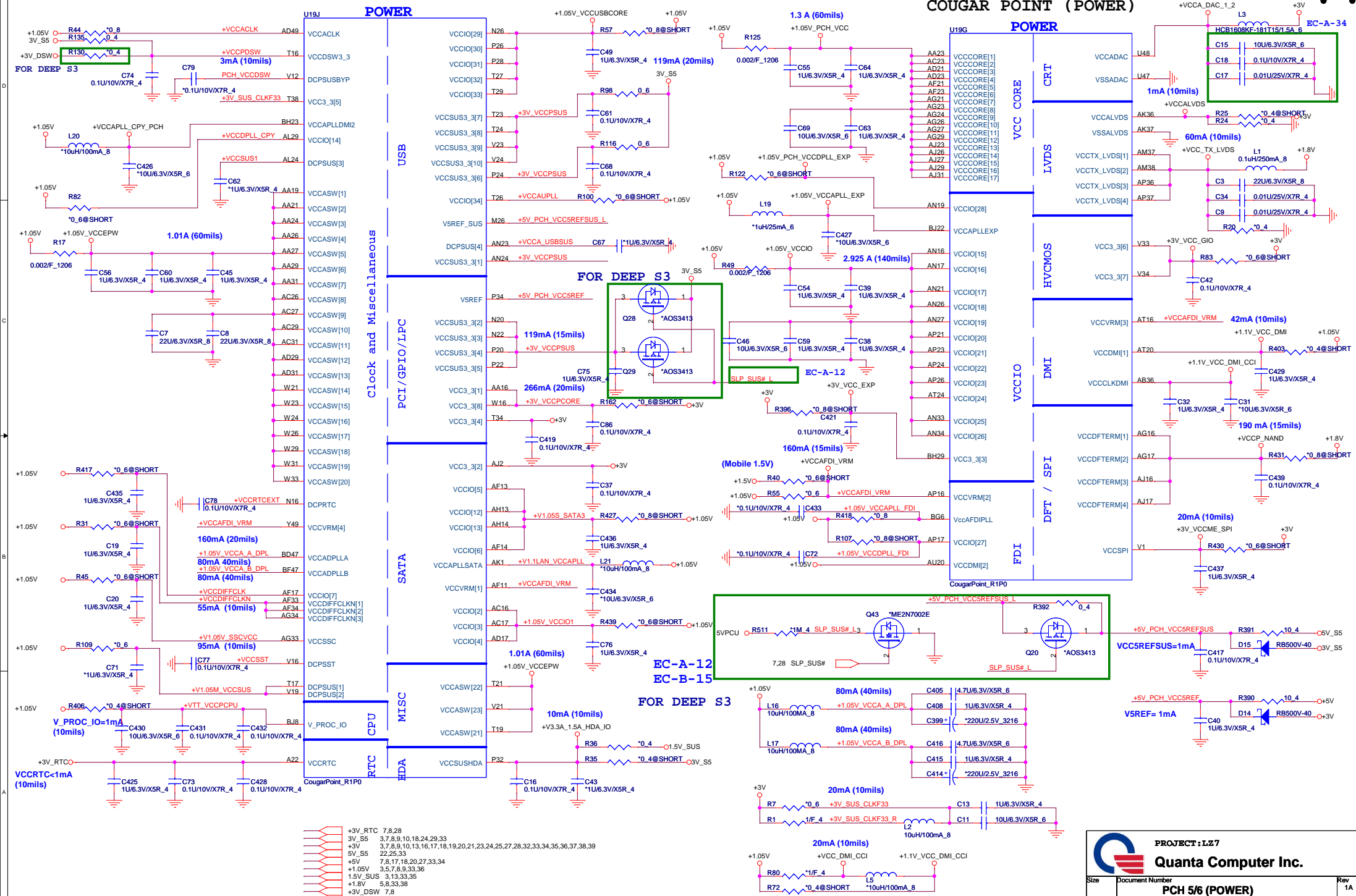
	SYSTEM_ID
L27	0
L28	1



PROJECT: L27
Quanta Computer Inc.

Size	Document Number	Rev
	PCH 4/6 (GPIO/MISC)	1A
Date:	Wednesday, December 21, 2011	Sheet 10 of 42

Cougar Point/Panther Point (POWER)



Cougar Point/Panther Point (GND)

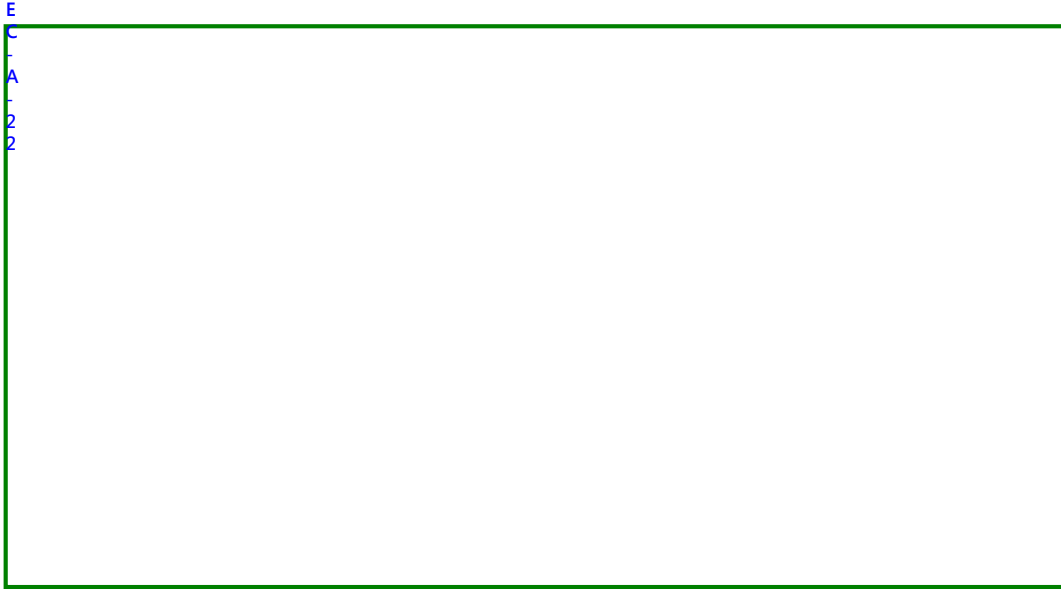
AY4	VSS[159]	VSS[259]	H46
AY42	VSS[160]	VSS[260]	K18
AY46	VSS[161]	VSS[261]	K26
AY8	VSS[162]	VSS[262]	K39
B11	VSS[163]	VSS[263]	K46
B15	VSS[164]	VSS[264]	K7
B19	VSS[165]	VSS[265]	L18
B23	VSS[166]	VSS[266]	L2
B27	VSS[167]	VSS[267]	L20
B31	VSS[168]	VSS[268]	L26
B35	VSS[169]	VSS[269]	L28
B39	VSS[170]	VSS[270]	L36
B7	VSS[171]	VSS[271]	L48
F45	VSS[172]	VSS[272]	M12
BB12	VSS[173]	VSS[273]	M18
BB16	VSS[174]	VSS[274]	M22
BB20	VSS[175]	VSS[275]	M24
BB22	VSS[176]	VSS[276]	M30
BB24	VSS[177]	VSS[277]	M32
BB28	VSS[178]	VSS[278]	M34
BB30	VSS[179]	VSS[279]	M38
BB38	VSS[180]	VSS[280]	M4
BB4	VSS[181]	VSS[281]	M42
BB46	VSS[182]	VSS[282]	M46
BC14	VSS[183]	VSS[283]	M8
BC18	VSS[184]	VSS[284]	N18
BC2	VSS[185]	VSS[285]	P30
BC22	VSS[186]	VSS[286]	P47
BC26	VSS[187]	VSS[287]	P7
BC32	VSS[188]	VSS[288]	R48
BC34	VSS[189]	VSS[289]	T12
BC36	VSS[190]	VSS[290]	T31
BC40	VSS[191]	VSS[291]	T4
BC42	VSS[192]	VSS[292]	W34
BC48	VSS[193]	VSS[293]	T46
BD46	VSS[194]	VSS[294]	T47
BD5	VSS[195]	VSS[295]	T8
BE22	VSS[196]	VSS[296]	V11
BE26	VSS[197]	VSS[297]	V17
BE40	VSS[198]	VSS[298]	V26
BE10	VSS[199]	VSS[299]	V27
BE12	VSS[200]	VSS[300]	V29
BE16	VSS[201]	VSS[301]	V31
BE20	VSS[202]	VSS[302]	V36
BE22	VSS[203]	VSS[303]	V39
BE24	VSS[204]	VSS[304]	V43
BE26	VSS[205]	VSS[305]	V7
BE28	VSS[206]	VSS[306]	W17
BD3	VSS[207]	VSS[307]	W19
BF40	VSS[208]	VSS[308]	W2
BF38	VSS[209]	VSS[309]	W27
BF40	VSS[210]	VSS[310]	W48
BF8	VSS[211]	VSS[311]	Y12
BG17	VSS[212]	VSS[312]	Y38
BG21	VSS[213]	VSS[313]	Y42
BG33	VSS[214]	VSS[314]	Y46
BG44	VSS[215]	VSS[315]	Y8
BG8	VSS[216]	VSS[316]	Y8
BH11	VSS[217]	VSS[317]	Y8
BH15	VSS[218]	VSS[318]	Y8
BH17	VSS[219]	VSS[319]	Y8
BH19	VSS[220]	VSS[320]	Y8
H10	VSS[221]	VSS[321]	Y8
BH27	VSS[222]	VSS[322]	Y8
BH31	VSS[223]	VSS[323]	Y8
BH33	VSS[224]	VSS[324]	Y8
BH35	VSS[225]	VSS[325]	Y8
BH39	VSS[226]	VSS[326]	Y8
BH43	VSS[227]	VSS[327]	Y8
BH7	VSS[228]	VSS[328]	Y8
D3	VSS[229]	VSS[329]	Y8
D12	VSS[230]	VSS[330]	Y8
D16	VSS[231]	VSS[331]	Y8
D18	VSS[232]	VSS[332]	Y8
D22	VSS[233]	VSS[333]	Y8
D24	VSS[234]	VSS[334]	Y8
D26	VSS[235]	VSS[335]	Y8
D30	VSS[236]	VSS[336]	Y8
D32	VSS[237]	VSS[337]	Y8
D34	VSS[238]	VSS[338]	Y8
D38	VSS[239]	VSS[339]	Y8
D42	VSS[240]	VSS[340]	Y8
D8	VSS[241]	VSS[341]	Y8
E18	VSS[242]	VSS[342]	Y8
E26	VSS[243]	VSS[343]	Y8
G18	VSS[244]	VSS[344]	Y8
G20	VSS[245]	VSS[345]	Y8
G26	VSS[246]	VSS[346]	Y8
G28	VSS[247]	VSS[347]	Y8
G36	VSS[248]	VSS[348]	Y8
G48	VSS[249]	VSS[349]	Y8
H12	VSS[250]	VSS[350]	Y8
H18	VSS[251]	VSS[351]	Y8
H22	VSS[252]	VSS[352]	Y8
H24	VSS[253]		
H26	VSS[254]		
H30	VSS[255]		
H32	VSS[256]		
H34	VSS[257]		
F3	VSS[258]		

CougarPoint_R1P0


Cougar Point/Panther Point (GND)

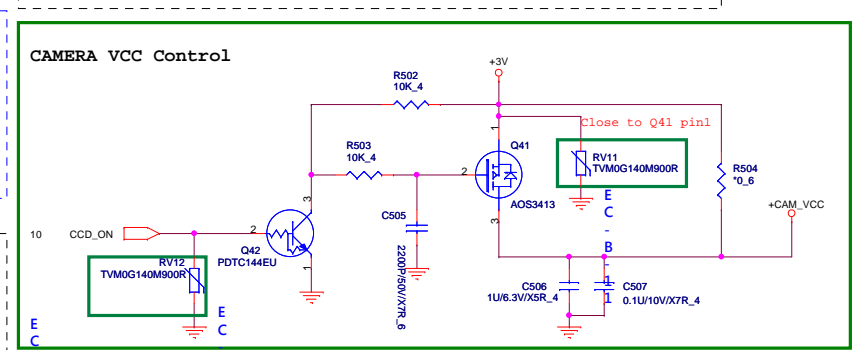
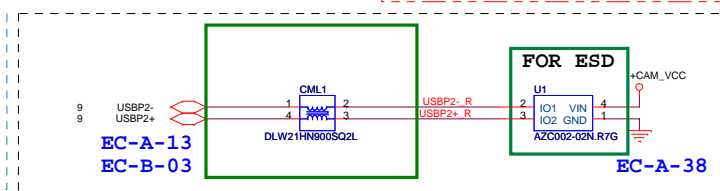
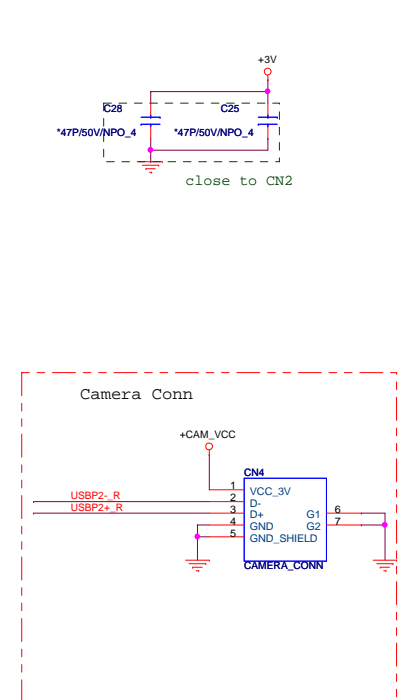
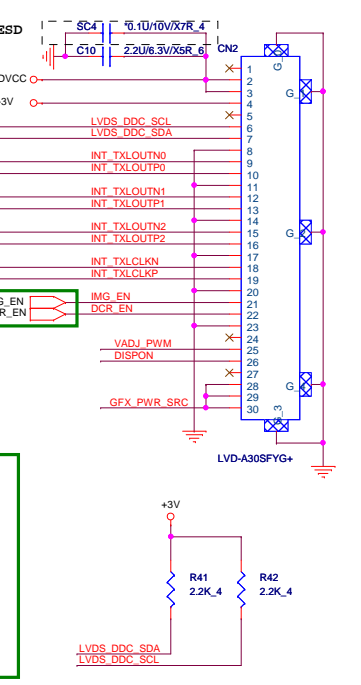
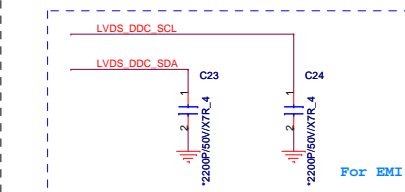
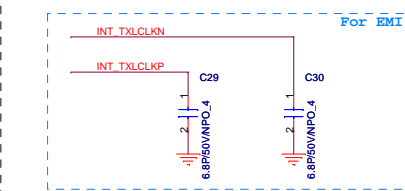
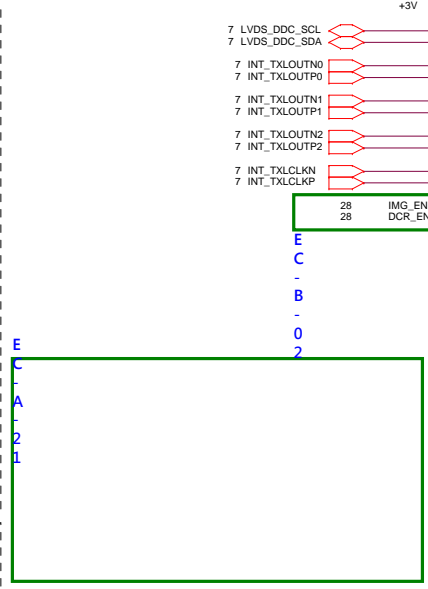
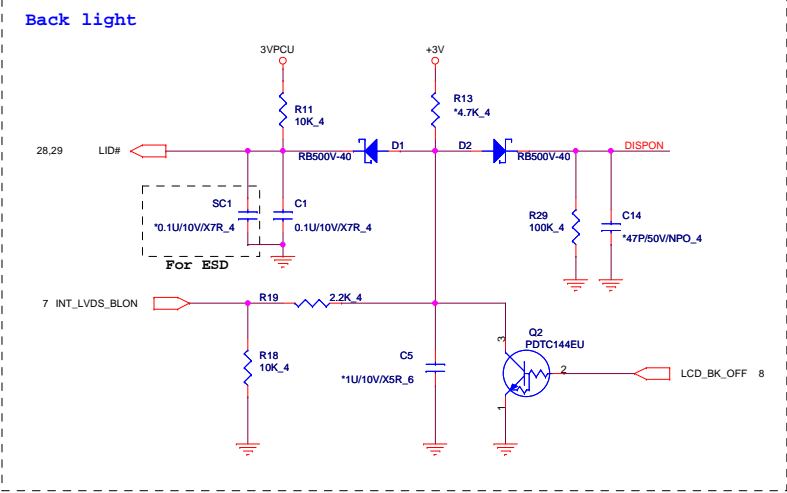
H5	VSS[0]	VSS[80]	AK38
AA17	VSS[1]	VSS[81]	AK4
AA2	VSS[2]	VSS[82]	AK42
AA3	VSS[3]	VSS[83]	AK46
AA33	VSS[4]	VSS[84]	AK8
AA34	VSS[5]	VSS[85]	AL16
AB11	VSS[6]	VSS[86]	AL17
AB3	VSS[7]	VSS[87]	AL19
AB4	VSS[8]	VSS[88]	AL2
AB43	VSS[9]	VSS[89]	AL21
AB5	VSS[10]	VSS[90]	AL23
AB7	VSS[11]	VSS[91]	AL26
AC19	VSS[12]	VSS[92]	AL27
AC2	VSS[13]	VSS[93]	AL31
AC21	VSS[14]	VSS[94]	AL33
AC24	VSS[15]	VSS[95]	AL34
AC33	VSS[16]	VSS[96]	AL48
AC34	VSS[17]	VSS[97]	AM11
AC48	VSS[18]	VSS[98]	AM14
AD10	VSS[19]	VSS[99]	AM36
AD11	VSS[20]	VSS[100]	AM39
AD12	VSS[21]	VSS[101]	AM43
AD13	VSS[22]	VSS[102]	AM45
AD19	VSS[23]	VSS[103]	AM46
AD24	VSS[24]	VSS[104]	AM7
AD26	VSS[25]	VSS[105]	AN2
AD27	VSS[26]	VSS[106]	AN29
AD33	VSS[27]	VSS[107]	AN3
AD34	VSS[28]	VSS[108]	AN31
AD36	VSS[29]	VSS[109]	AP12
AD37	VSS[30]	VSS[110]	AP19
AD38	VSS[31]	VSS[111]	AP28
AD39	VSS[32]	VSS[112]	AP30
AD4	VSS[33]	VSS[113]	AP32
AD40	VSS[34]	VSS[114]	AP38
AD42	VSS[35]	VSS[115]	AP4
AD43	VSS[36]	VSS[116]	AP42
AD45	VSS[37]	VSS[117]	AP46
AD46	VSS[38]	VSS[118]	AP8
AD8	VSS[39]	VSS[119]	AR2
AE2	VSS[40]	VSS[120]	AR48
AE3	VSS[41]	VSS[121]	AT11
AE10	VSS[42]	VSS[122]	AT13
AF12	VSS[43]	VSS[123]	AT18
AD14	VSS[44]	VSS[124]	AT22
AD16	VSS[45]	VSS[125]	AT26
AF16	VSS[46]	VSS[126]	AT28
AF19	VSS[47]	VSS[127]	AT30
AF24	VSS[48]	VSS[128]	AT32
AF26	VSS[49]	VSS[129]	AT34
AF27	VSS[50]	VSS[130]	AT39
AF28	VSS[51]	VSS[131]	AT42
AF31	VSS[52]	VSS[132]	AT46
AF36	VSS[53]	VSS[133]	AT7
AF38	VSS[54]	VSS[134]	AU24
AF4	VSS[55]	VSS[135]	AU30
AF42	VSS[56]	VSS[136]	AV16
AF46	VSS[57]	VSS[137]	AV20
AF5	VSS[58]	VSS[138]	AV24
AF7	VSS[59]	VSS[139]	AV30
AF8	VSS[60]	VSS[140]	AV38
AG19	VSS[61]	VSS[141]	AV4
AG2	VSS[62]	VSS[142]	AV43
AG31	VSS[63]	VSS[143]	AV8
AG48	VSS[64]	VSS[144]	AW14
AH11	VSS[65]	VSS[145]	AW18
AH3	VSS[66]	VSS[146]	AW2
AH36	VSS[67]	VSS[147]	AW22
B43	VSS[68]	VSS[148]	AW26
BE10	VSS[69]	VSS[149]	AW28
AH42	VSS[70]	VSS[150]	AW32
AH46	VSS[71]	VSS[151]	AW34
AH7	VSS[72]	VSS[152]	AW36
AJ19	VSS[73]	VSS[153]	AW40
AJ21	VSS[74]	VSS[154]	AW48
AJ24	VSS[75]	VSS[155]	AV11
AJ33	VSS[76]	VSS[156]	AV12
AJ34	VSS[77]	VSS[157]	AY22
AK12	VSS[78]	VSS[158]	AY28
AK3	VSS[79]		

CougarPoint_R1P0

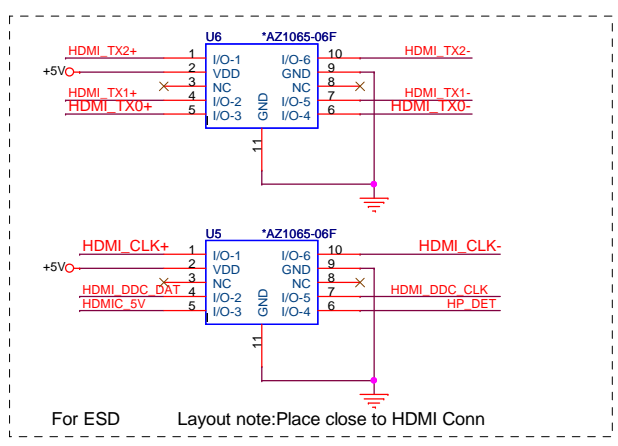
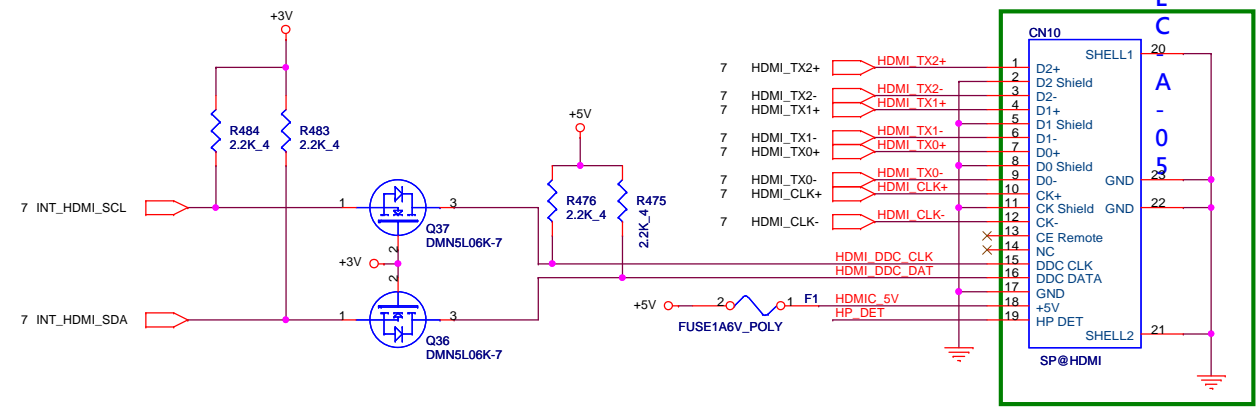
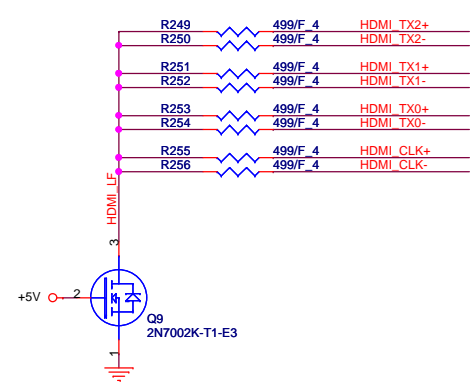


E
C
A
2
2

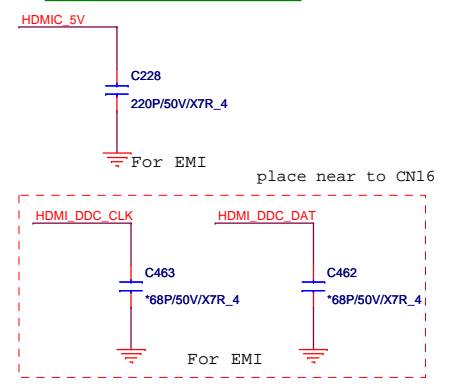
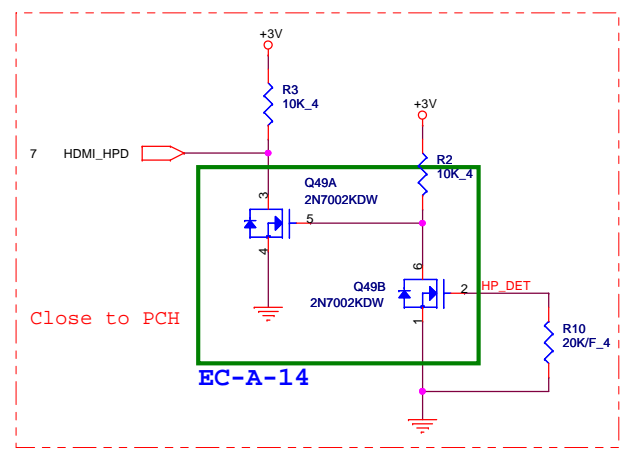
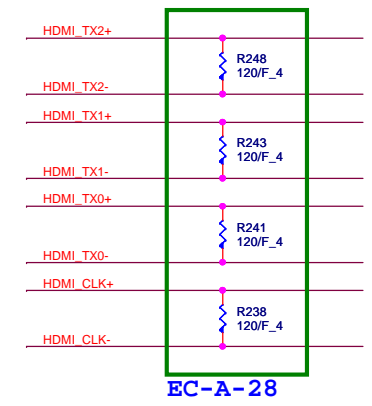
		PROJECT: LZ7	
		Quanta Computer Inc.	
Size	Custom	Document Number	Rev
		Blank	
Date:	Wednesday, December 21, 2011		Sheet 15 of 42



3,7,8,9,10,11,13,16,18,19,20,21,23,24,25,27,28,32,33,34,35,36,37,38,39 +3V
7,8,11,18,20,27,33,34 +5V

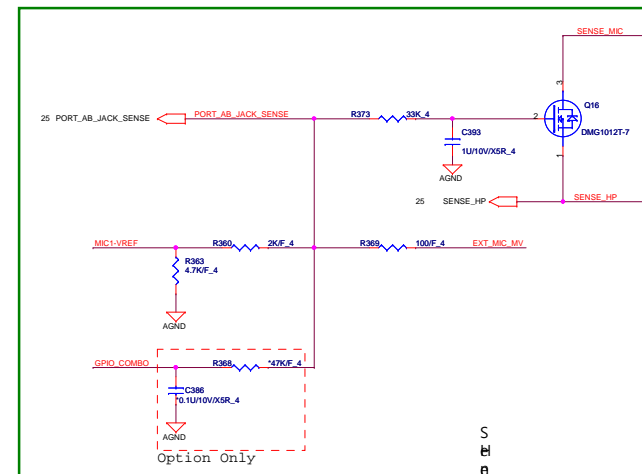


EMI reserve for HDMI

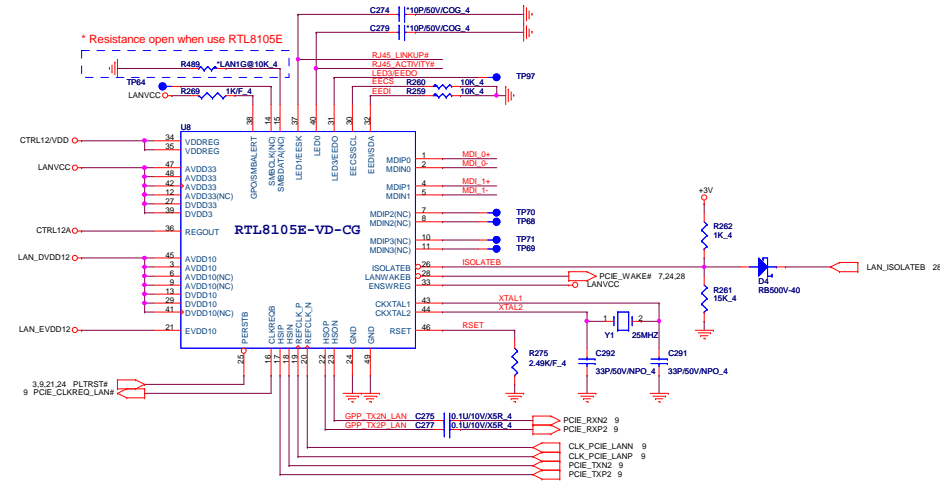
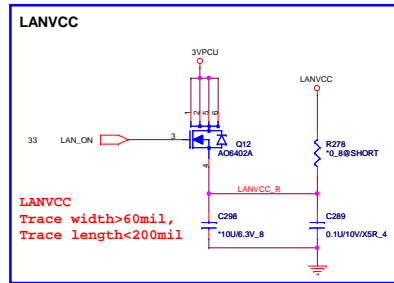


AVDD_3.3 pin is output of internal LDO. Do NOT connect to external supply.

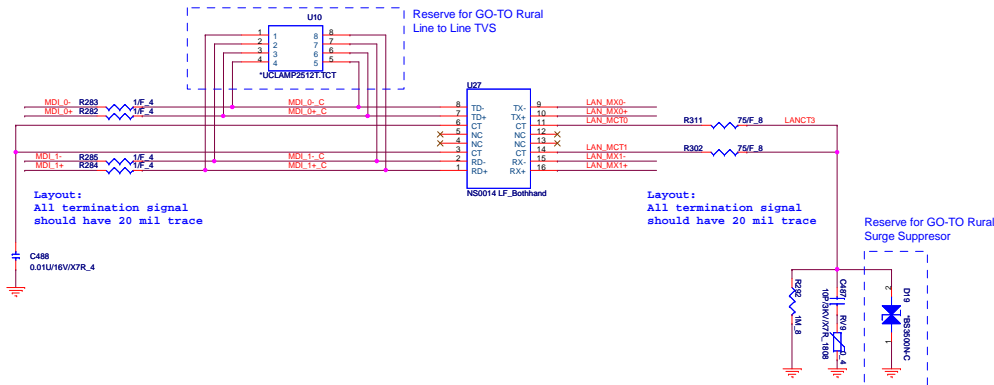
Conexant FAE Suggest when use intel HDA interface



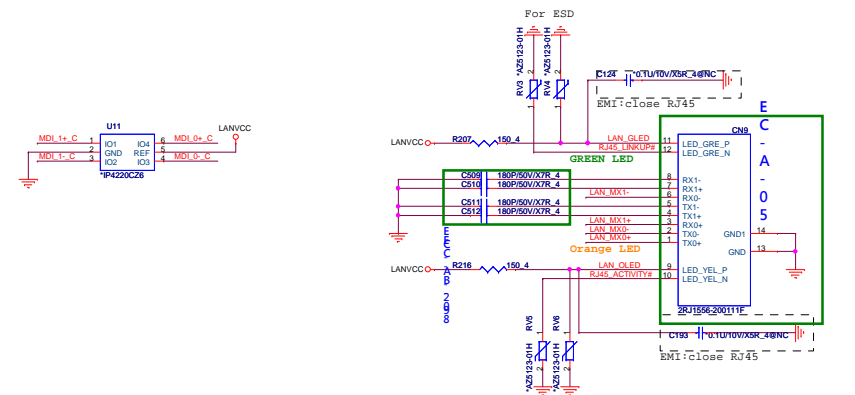
8
e
P
P
C
n
e
M
E
C
X

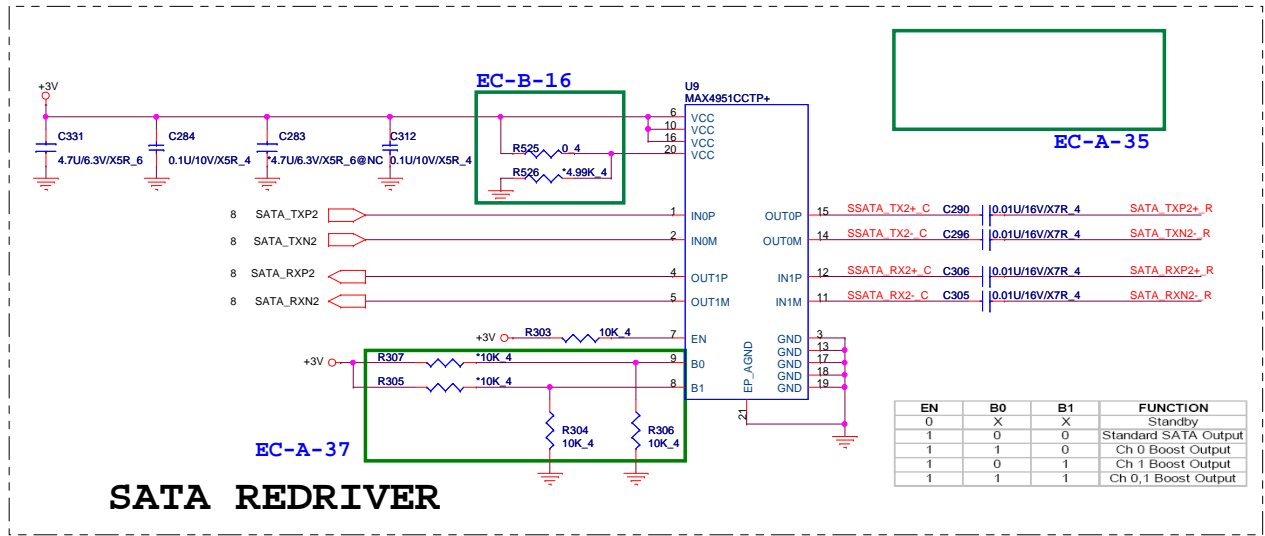
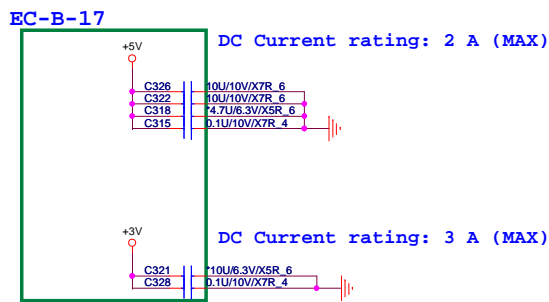
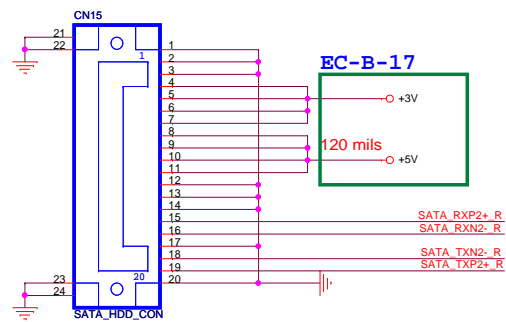



Transformer



RJ45 Connector





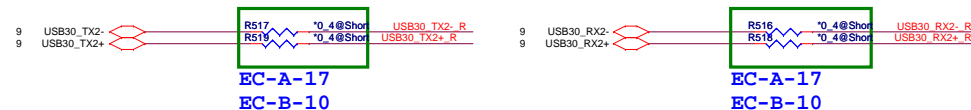
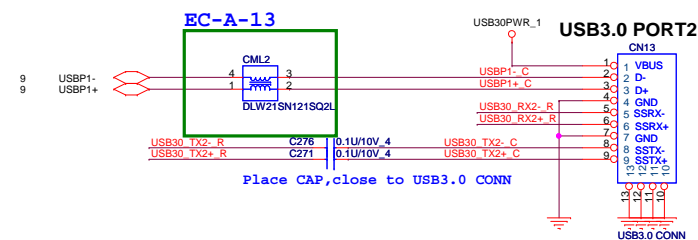
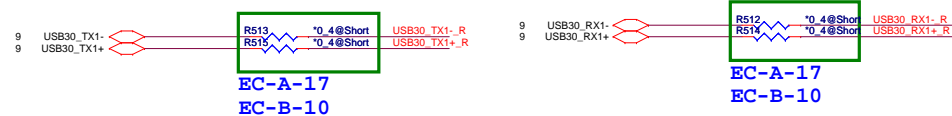
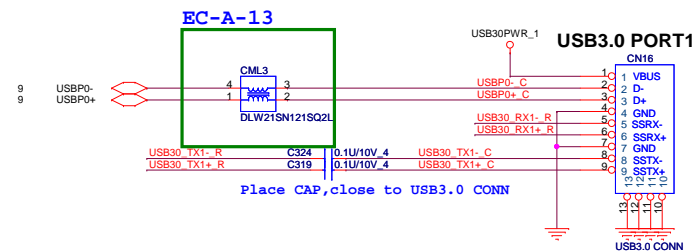
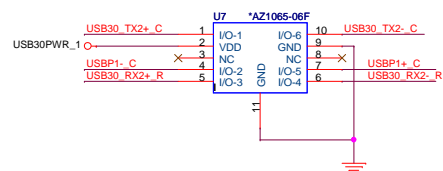


PROJECT: LZ7

Quanta Computer Inc.

Size	Document Number	Rev
	SATA	1A
Date:	Wednesday, December 21, 2011	Sheet 20 of 42

21

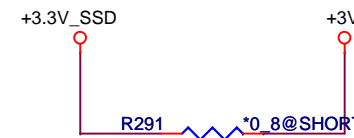
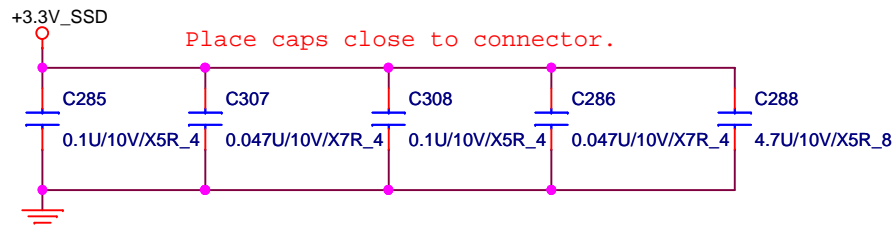
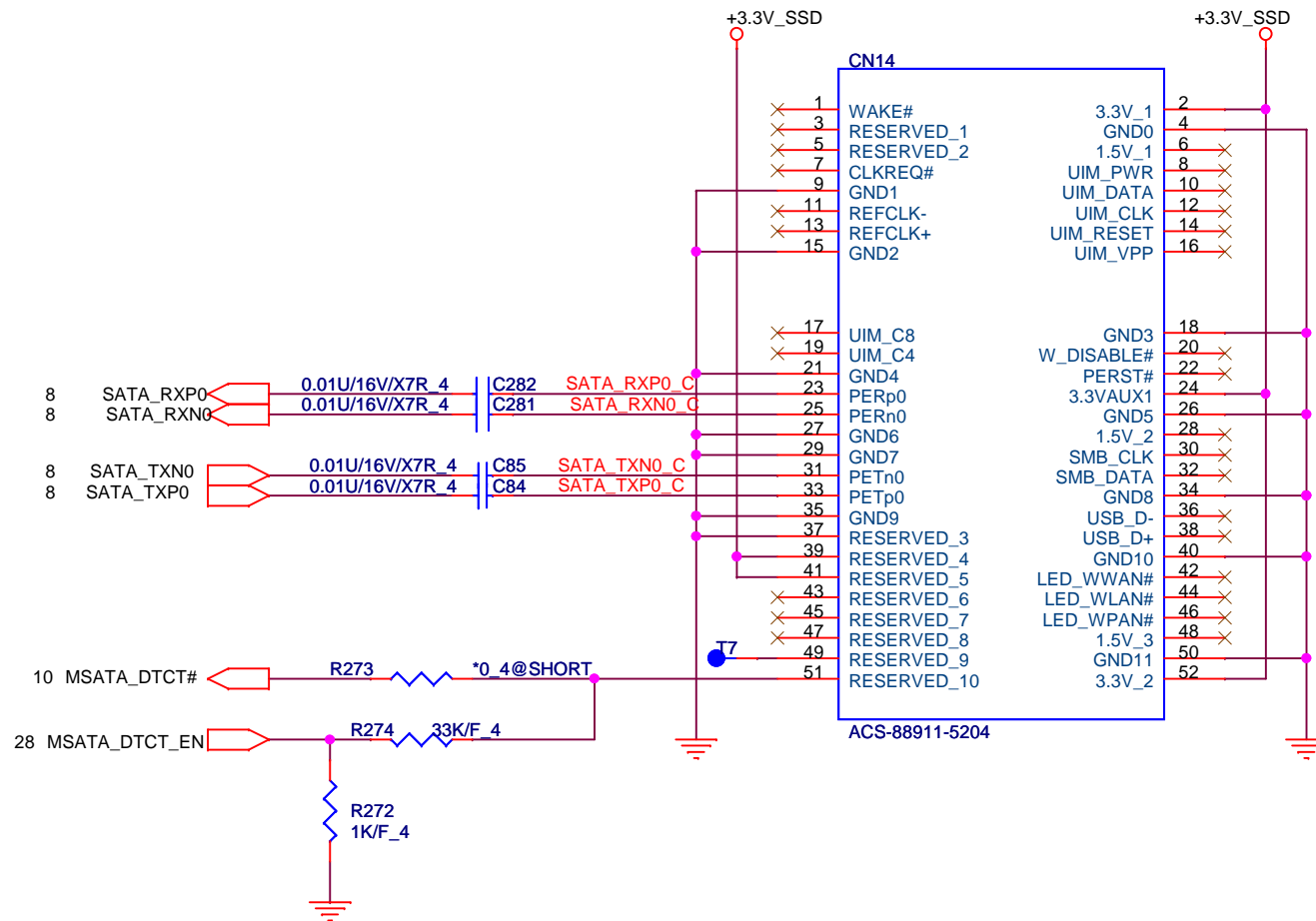


Mini PCI-E Card SSD

3,7,8,9,10,11,13,16,17,18,19,20,21,24,25,27,28,32,33,34,35,36,37,38,39
11,24,35

+3V
+1.5V


23



		PROJECT: LZ7	
		Quanta Computer Inc.	
Size Custom	Document Number		Rev 1E
		MINI Card (SSD)	
Date:	Wednesday, December 21, 2011	Sheet	23 of 42



	5	4	3	2	1
D					
C					
B					
A					



PROJECT : LZ7

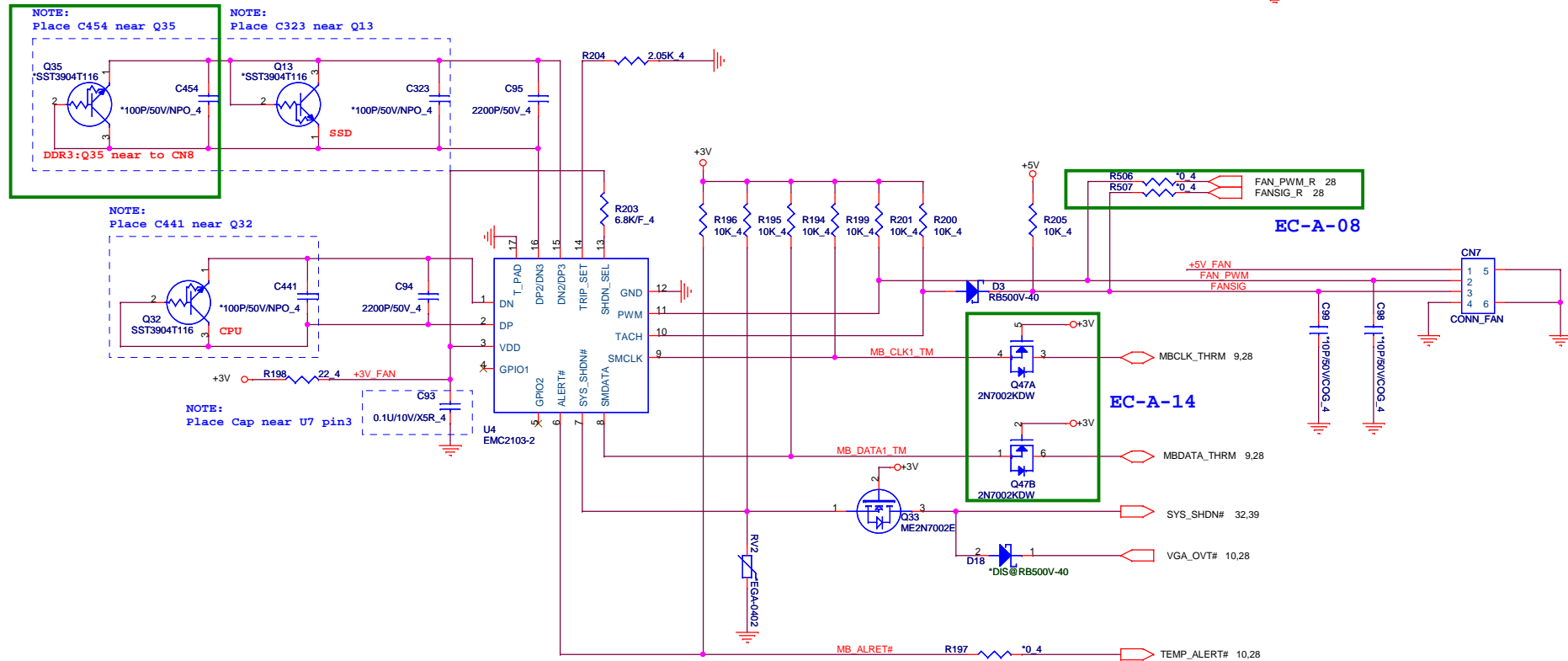
Quanta Computer Inc.

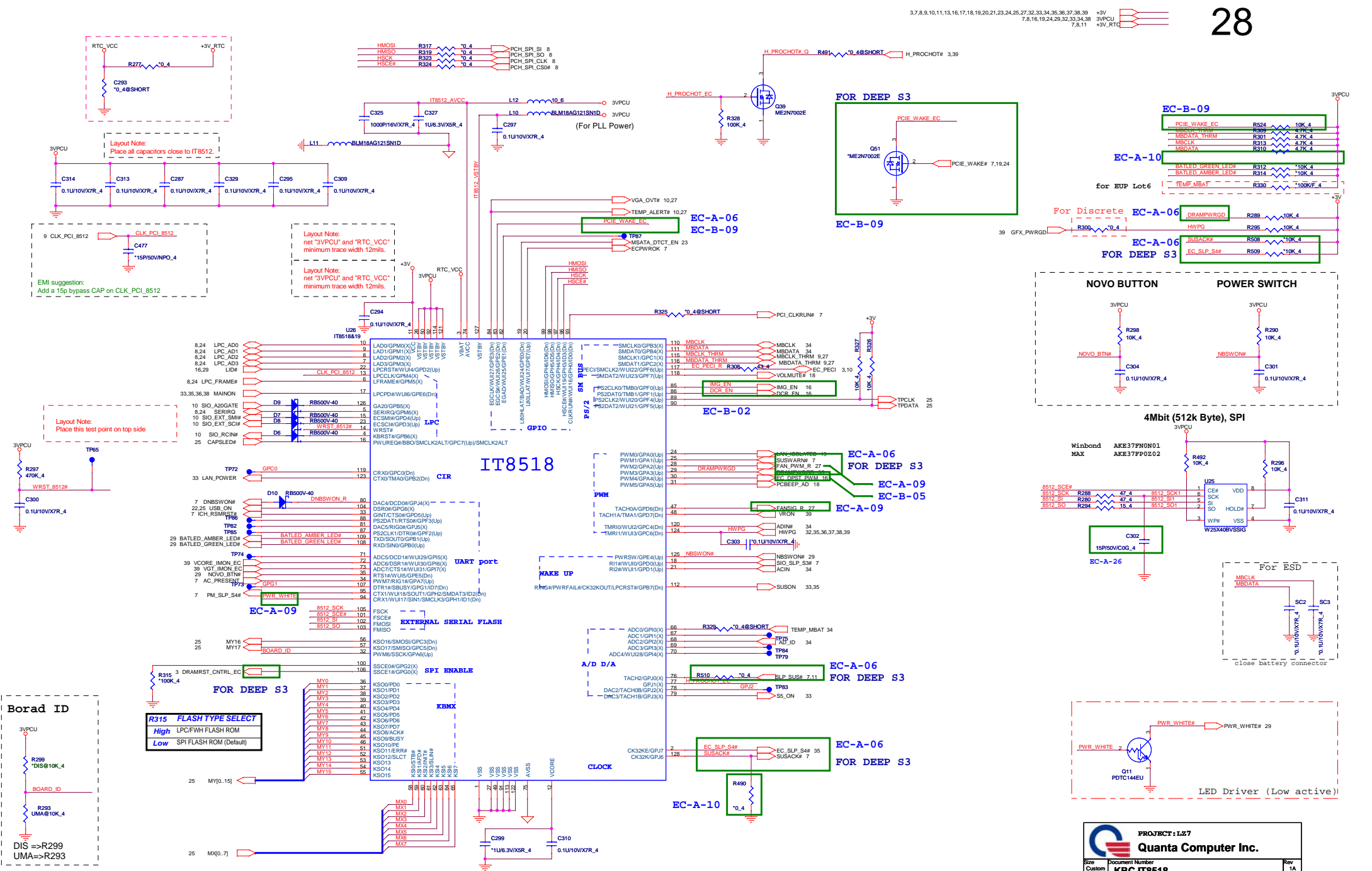
Size	Document Number	Rev
	BLANK	1A
Date:	Wednesday, December 21, 2011	Sheet 26 of 42

3,7,8,9,10,11,13,16,17,18,19,20,21,23,24,25,28,32,33,34,35,36,37,38,39 +3V
7,8,11,17,18,20,33,34 +5V

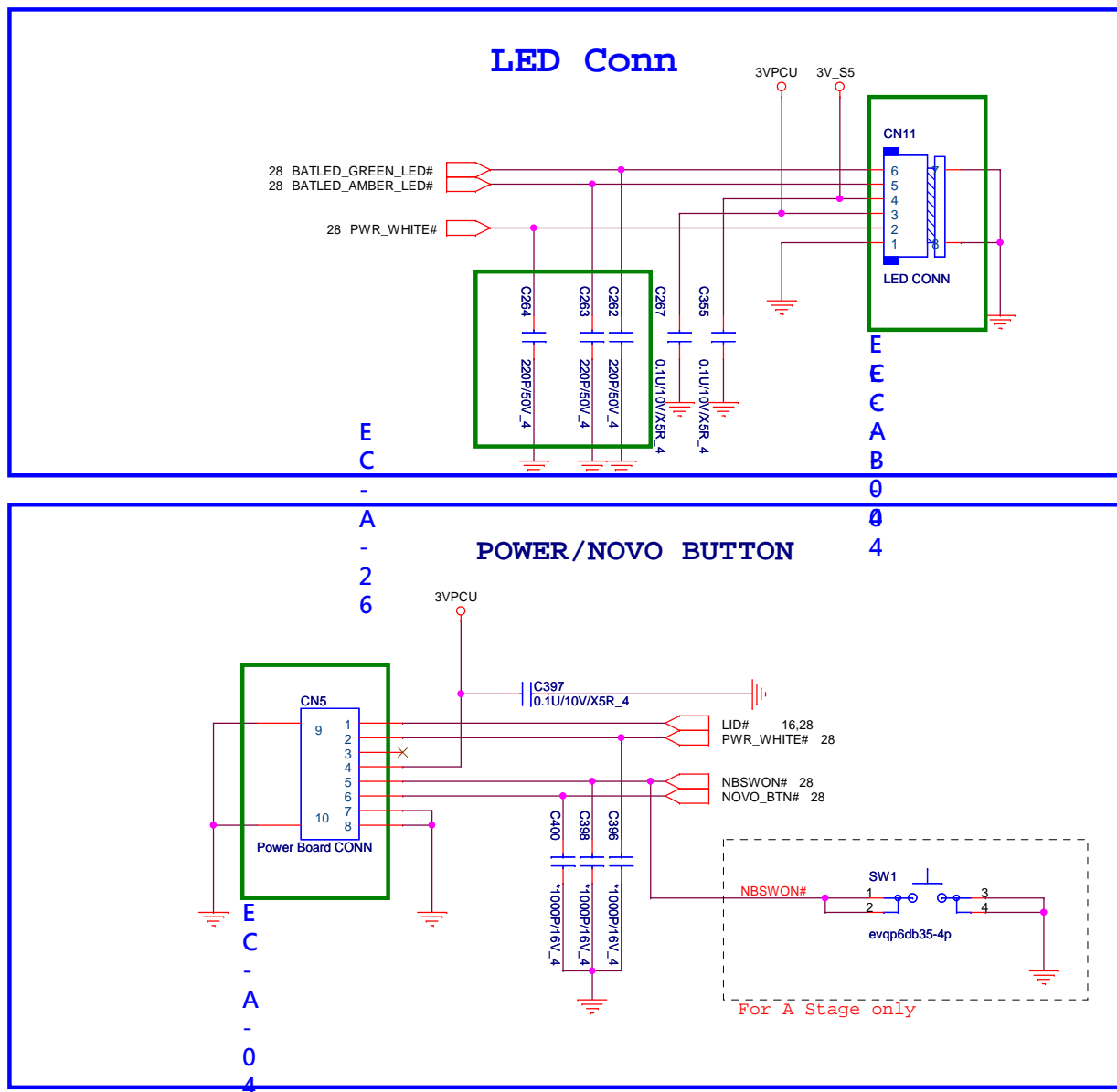


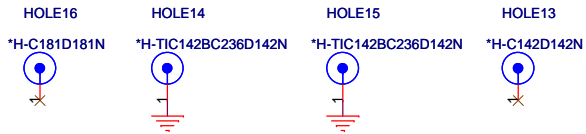
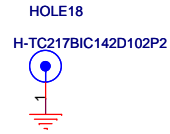
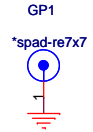
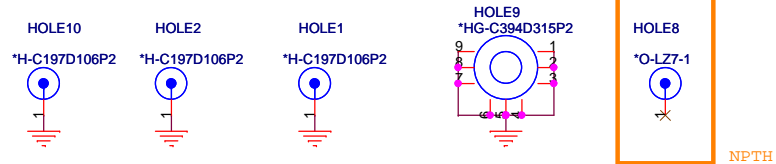
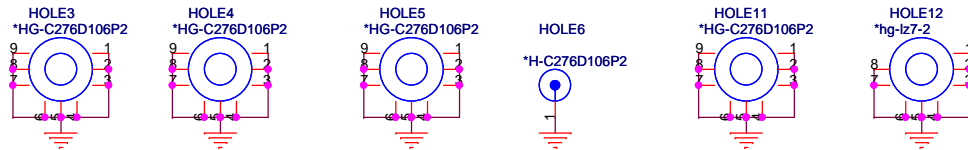
EC-B-07
EC-A-25





+3V	3,7,8,9,10,11,13,16,17,18,19,20,21,23,24,25,27,28,32,33,34,35,36,37,38,39
3VPCU	7,8,16,19,24,28,32,33,34,38
3V_S5	3,7,8,9,10,11,18,24,33



Hole for CPU support**MiniCard SSD****MiniCard WLAN****PAD****Boundary Hole****Round screw hole**

PROJECT : LZ7

Quanta Computer Inc.

Size

Document Number

Rev

Screw Hole/EMI

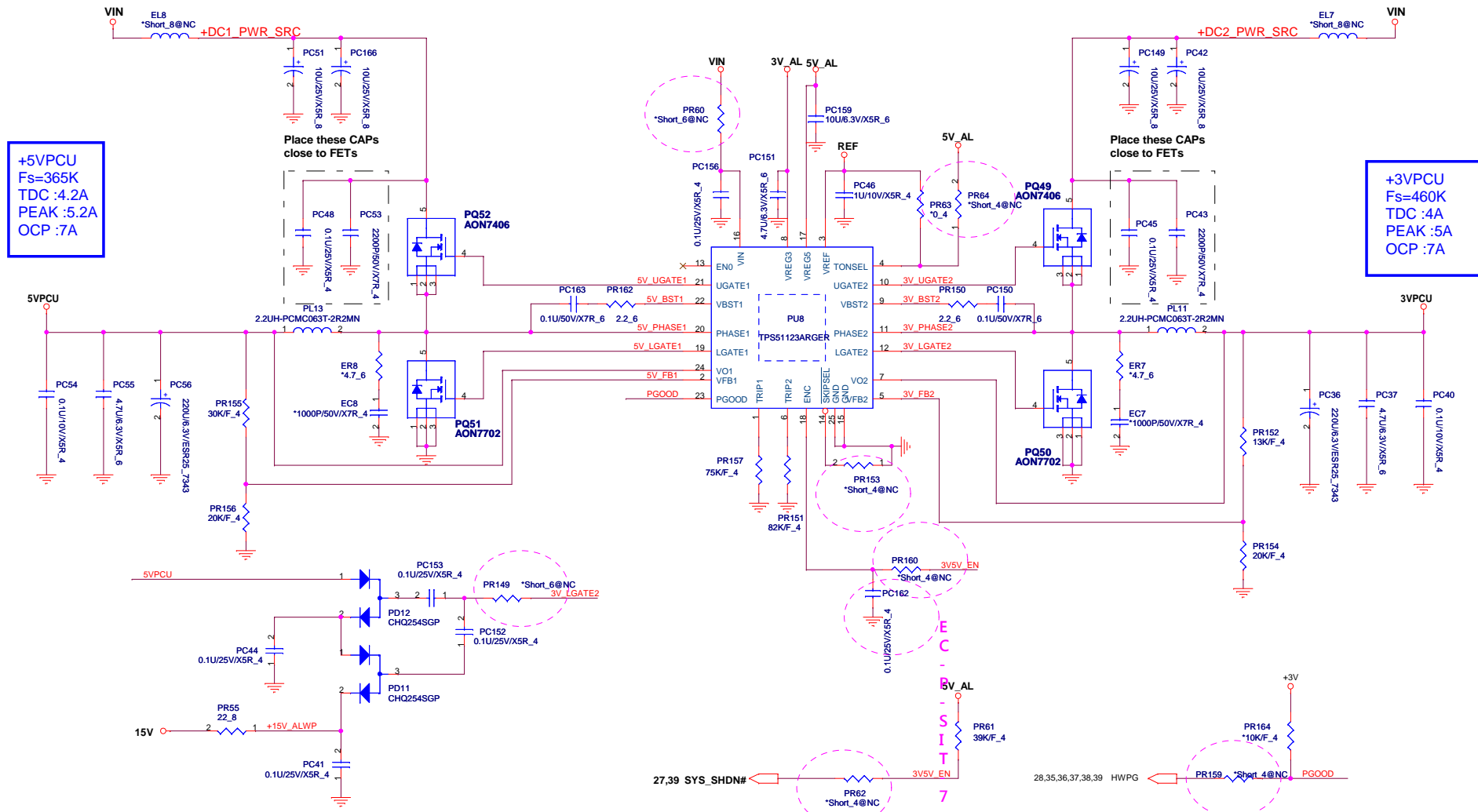
1A

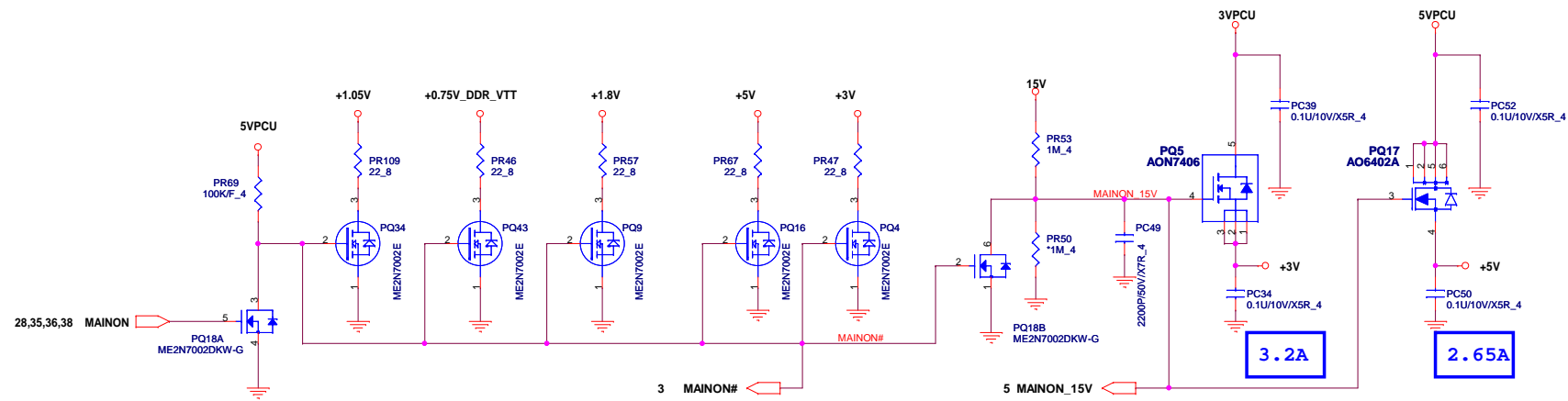
Date: Wednesday, December 21, 2011

Sheet 30 of 42

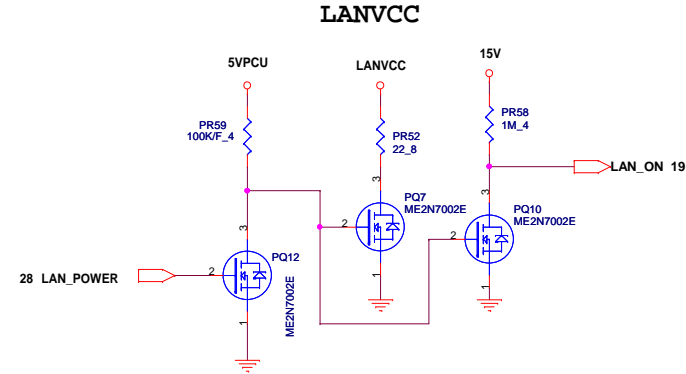
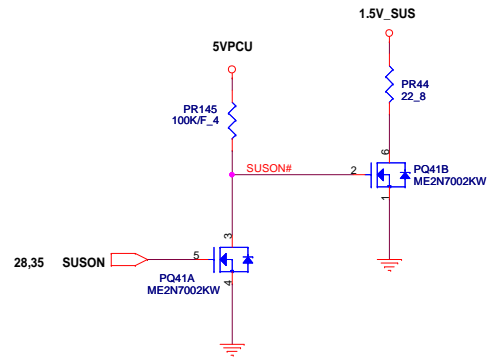
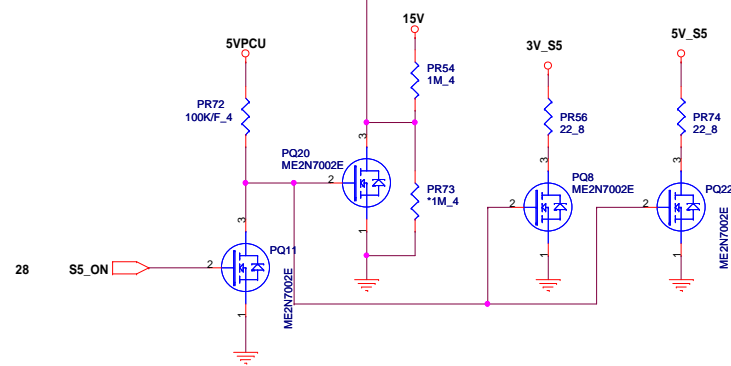
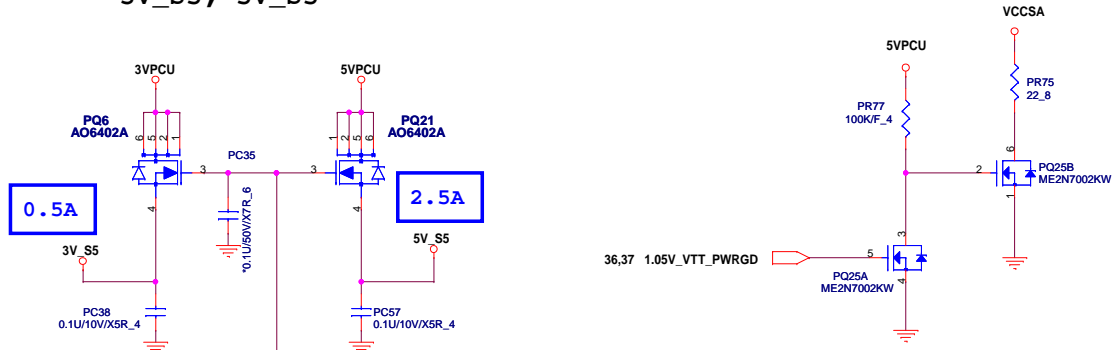
7

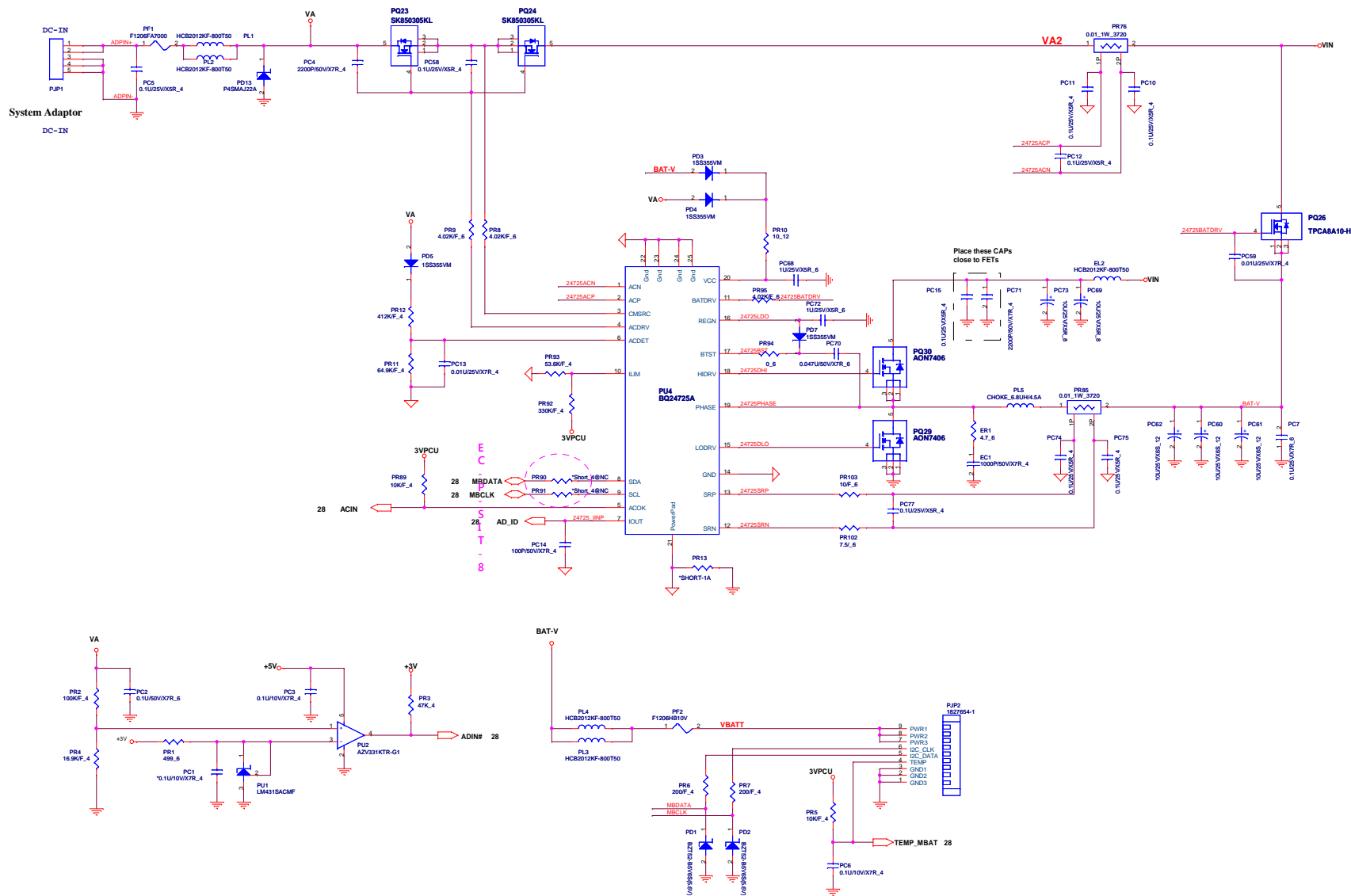
8



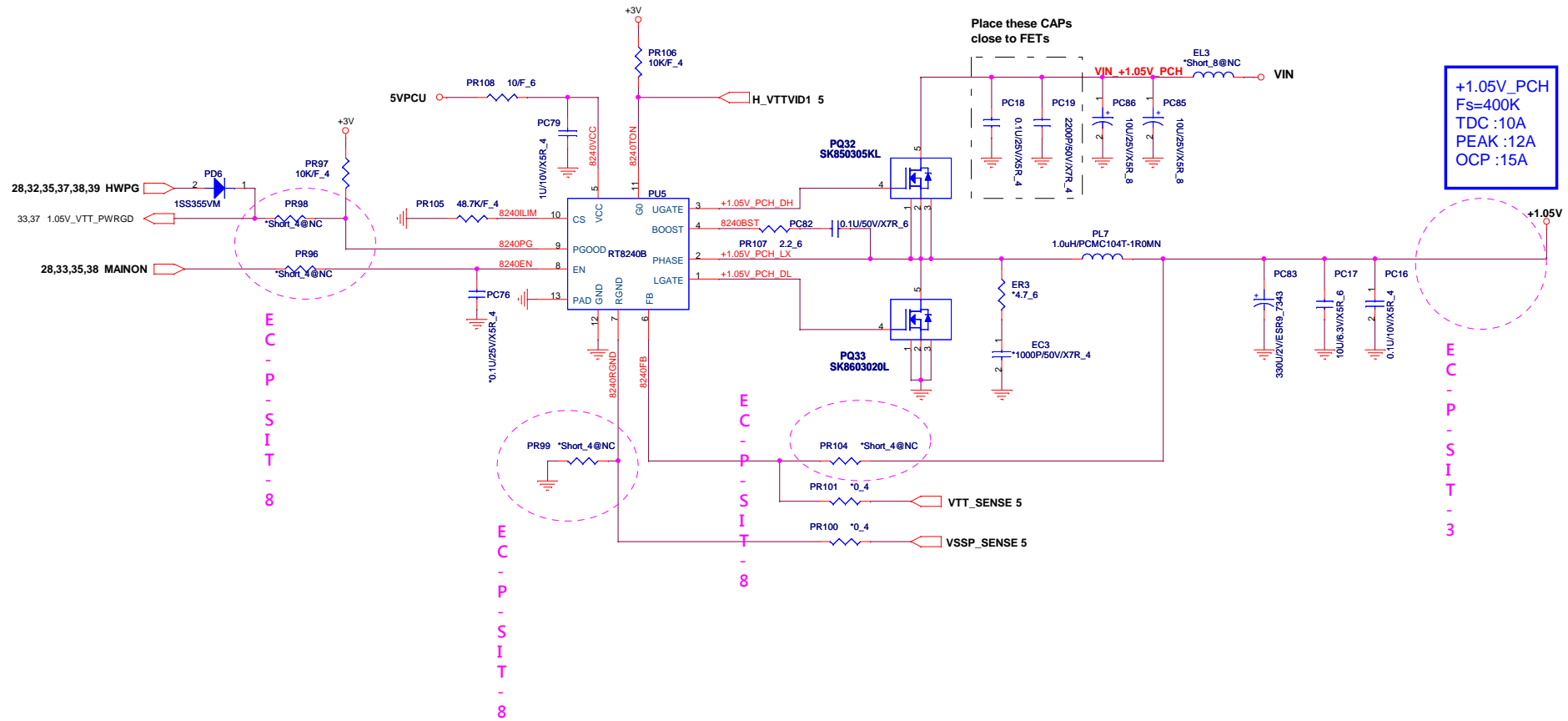


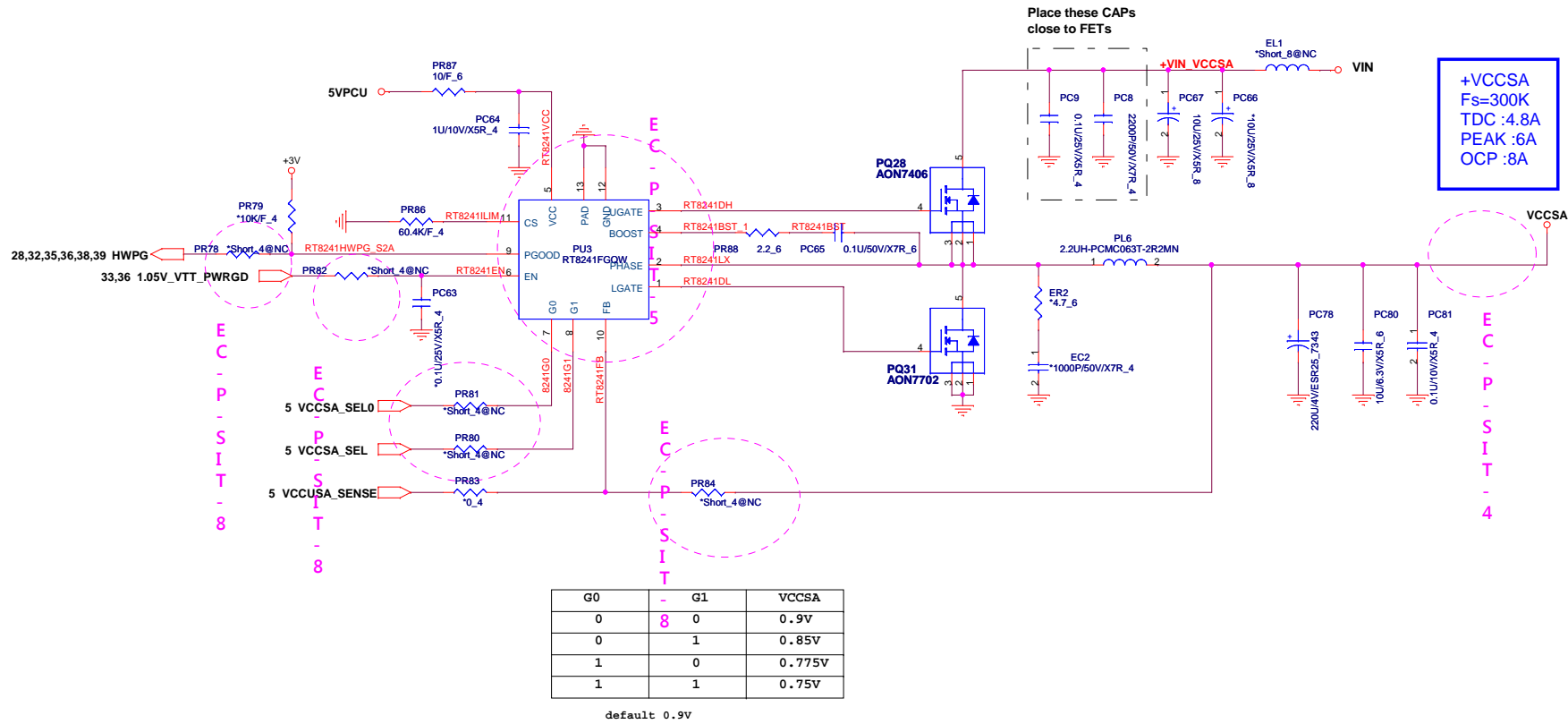
3V_S5, 5V_S5



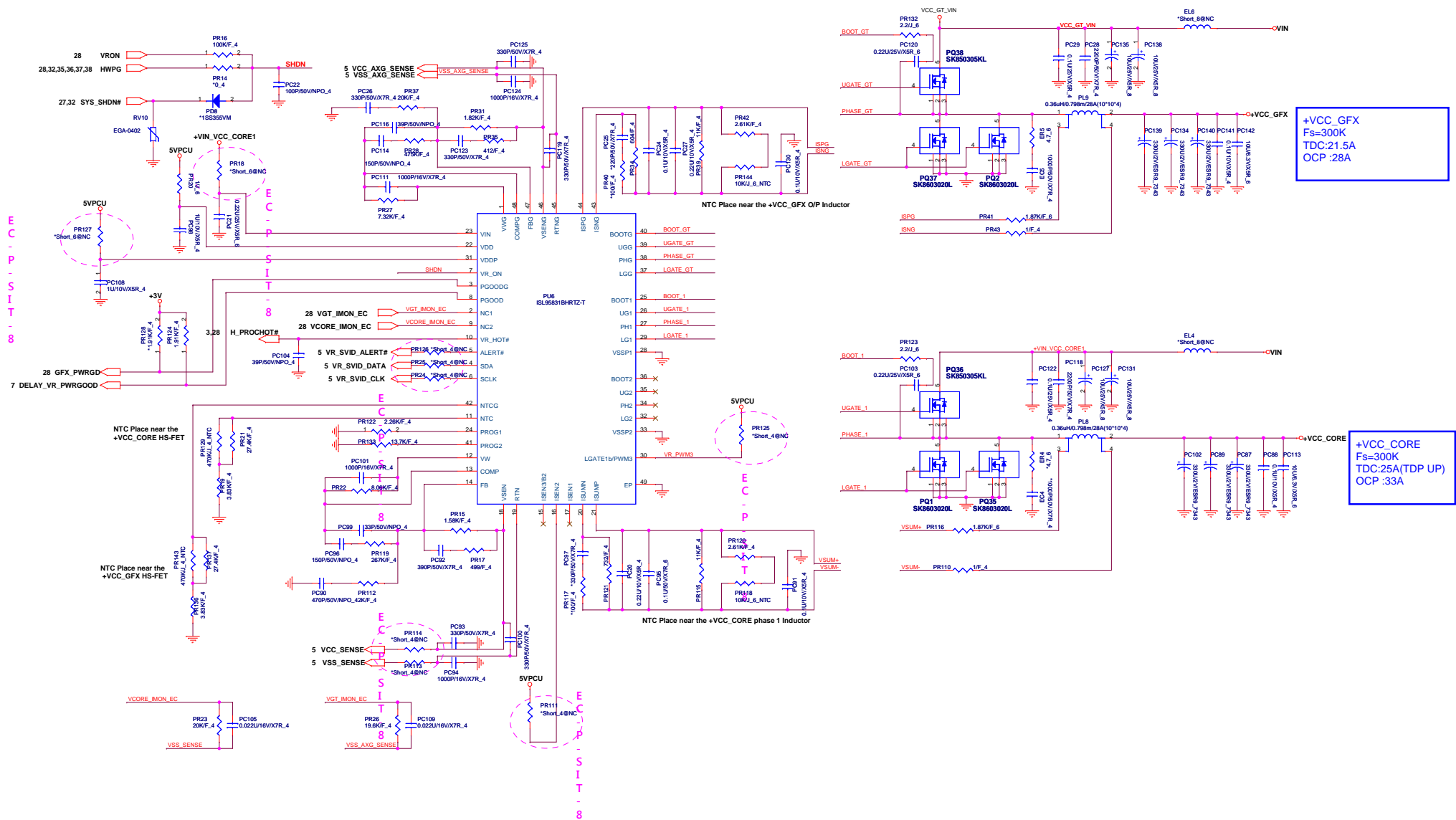








+VCCSA
Fs=300K
TDC :4.8A
PEAK :6A
OCP :8A



E C N	P G	D A/mm/dd	P A	D E S C R I P T I O N
EC-A-01	10,16	11/10/04	C505,C506,C507,Q41,Q42,R502,R503,R504	change GPIO35 to CCD_ON for bios request, Add camera control circuit
EC-A-02	18	11/10/11	Q16,R373,C393,R360,R369,R368,C386,U17	modify audio combo jack circuit for audio plug in/out nosie
EC-A-03	25	11/10/11	CN18,C348,C356,C352	Delete C348,C356,R352 change CN18 Pin define
EC-A-04	29	11/10/12	CN5,CN11	Change CN5,CN11 footprint from pitch 1.0mm to 0.5mm
EC-A-05	17,19	11/10/12	CN10,CN9	Change CN9,CN10 footprint to correct one
EC-A-06	7,28	11/10/17	C508,R509,R112	Add DEEP S3 function
EC-A-07	10	11/10/17	R88,R93	R93 Asm,R88 noAsm for Change Board ID to SIV stage
EC-A-08	27	11/10/17		Add EC detect Fan speed circuit
EC-A-09	28	11/10/17		Change EC pin define,PIN94 connect to PWR_WHITE,PIN28 connect to FAN_PWM_R,PIN47 connect to FANSIG_R
EC-A-10	28	11/10/17	R316,R490	Del R316 for pin94 use PWR WHITE signal No Asm R490 for EC use internal clock
EC-A-11	24	11/10/17	Q14,R331	Q14 Asm,R331 No Asm for input AOAC function
EC-A-12	11	11/10/17		Add DEEP S3 function
EC-A-13	16,22,25	11/10/17	CML1,CML2,CML3,CML4,R320,R318,R271,R270	CML2,CML3 CML4 asm R320,R318,R271,R270 R345,R346 noasm for EMI request Change common choke footprint from CHOKENCCM20C900-TR-4P to choke-dlw21s-4p for SMT request
EC-A-14	9,16,27	11/10/17	Q25,Q24,Q26,Q27,Q31,Q34,Q44,Q45,Q49,Q47,Q3,Q5	del Q25,Q24,Q26,Q27,Q31,Q34,Q3,Q5 Add Q44,Q45,Q47,Q49 change from mos to Dual mos(sot363)
EC-A-15	24	11/10/17	C489	Change footprint from CH6101K9A14 0805 to CH6101M1904 0603 for ME Height limit
EC-A-16	7	11/10/18	R185	R185 asm for System PWR_OK tune
EC-A-17	22	11/10/18	CML5,6,7,8 R512,R513,R514,R515,R516,R517,R518,R519	Reserve CML5,6,7,8 R512,R513,R514,R515,R516,R517,R518,R519 asm for EMI request
EC-A-18	5	11/10/19	C508	Add 10uF 6.3V Cap on VCCSA for INTEL DG request
EC-A-19	7	11/10/21	R4,R5,R6,R379,R380,R381	Delete Reserve LVDS signal from PCH
EC-A-20	8	11/10/21		Delete SATA2 for PCH Change to HM77
EC-A-21	25	11/10/21		Change CN6 footprint from GB1RF260-1253-8F to 88513-2641-26p-1-smt for SMT request
EC-A-22	15	11/10/21	C21,C22,C33,C35,C44,C48,C50,C51,C52,C58,C65,C66,C87,C418,C420,C424,L4,L6,L7,L18,Q19,Q48,Q48,R48,R53,R60,R61,R63,R64,R66,R68,R75,R81,R94,R95,R96,R97,R103,R385,R393,U2,U18	Delete eDP to LVDS IC Page
EC-A-23	3	11/10/21	RP7,R447,R448,R467,C449,C450,C453,C452	R467,RP7 no asm , R447,R448 asm for eDP function disable
EC-A-24	3	11/10/21	R478,U23,R482,Q38,R120,R477	R478,R482,Q38 asm ,U23,R120,R477 Noasm Delete AND GATE for intel CRB Suggest
EC-A-25	27	11/10/21	Q35	Add Q35 for thermal request
EC-A-26	18,28,29	11/10/22	C406,C407,C410,C411,C302,C262,C263,C264	audio C406,C407,C410,C411(CH4102K1B03)asm EC C302(CH01506JBD9)asm LED C262,C263,C264(CH12206JB00)asm for EMI request
EC-A-27	25	11/10/22	CA1,CA2,CA3,CA4,CA5	CA1,2,3,4,5 asm for KB EMI request
EC-A-28	17	11/10/22	R248,R243,R241,R238	R248,R243,R241,R238 asm for HDMI EMI request
EC-A-29	19	11/10/24	C509,C510,C511,C512	Reserve C509,C510,C511,C512 for LAN EMI request
EC-A-30	18	11/10/24	R386,R387,R388,R389,R366,C387	R386,R387,R388,R389 change to CX8PG181001 R366 Change to CX471T10000 C387 Change to CH0226F0B05 for EMI request
EC-A-31	25	11/10/24	CA6,C513,C514,C515,C516	delete CA6 and change from cap array to cap 0402 C513,C514,C515,C516 asm for EMI request
EC-A-32	8	11/10/24	R84,C369	Change R84 to CS02202FB12 change C369 to CH01506JBD9 for EMI request
EC-A-33	22	11/10/24	U24	Change U24 from G547E2P81U to G547N1P81U for 3.7A usb3.0 2 port Current
EC-A-34	11	11/10/24	C15,C17,C18	C15,C17,C18 asm for VCCDAC ripple voltage issue
EC-A-35	20	11/10/27		Del R276,R279,R281,R287 for SATA TX RX Signal line Branch too long issue
EC-A-36	18	11/10/27	C383,C363,C351,C365,C353,C352	C383,C363,C351,C365,C353,C352 noasm for FAE Suggest
EC-A-37	20	11/10/27	R307,R305	R307,R305 No asm , for Boost mode change to Standard mode
EC-A-38	16,25	11/10/31	U1,RV7,RV8	U1,RV7,RV8 asm , for ESD request

[illegible]

EC NO.	PG.	DATE	PART REFERENCE	DESCRIPTION
EC-P-SIV-1	32		PR157,PR151	3VPCU,5VPCU OCP set
EC-P-SIV-2	34		PJP1	Change DC-IN CONN footprint
EC-P-SIV-3	34		PF1,PF2	Change Fuse footprint
EC-P-SIV-4	34		PQ26	Change N-MOSFET with built-in Schottky diode
EC-P-SIV-5	34		EL2	Add charger bead
EC-P-SIV-6	34		PR85	Change PR85 to 10mohm
EC-P-SIV-7	34		PR13	Change PR13 footprint
EC-P-SIV-8	34		PR11,PR12	Change ACDET voltage
EC-P-SIV-9	34		PR92,PR93	Change ILIM voltage
EC-P-SIV-10	34			Modify MBDATA,MBCLK
EC-P-SIV-11	35		PJP8,PJP9	Change to default short
EC-P-SIV-12	35		PC144	Change to NC
EC-P-SIV-13	35		PR32	Change PR32 footprint
EC-P-SIV-14	35			Change PU7 GND
EC-P-SIV-15	35		PR138	Change PR138 for 1.5V regulation
EC-P-SIV-16	35		PD14	Add PD14 for S3
EC-P-SIV-17	35		PJP6	Change to default short
EC-P-SIV-18	35			Change netname for EE request
EC-P-SIV-19	36		PJP3,PJP4	Change to default short
EC-P-SIV-20	36		PR105	Change PR105 to 48.7K for OCP set
EC-P-SIV-21	36		PR99,PR100 PR101,PR104	Change PR99 & PR100 to 0ohm,Change PR101 & PR104 to NC
EC-P-SIV-22	37		PJP5	Change to default short
EC-P-SIV-23	37		PR86	Change PR86 to 60.4K for OCP set
EC-P-SIV-24	37		PR83,PR84	Change PR84 to 0ohm,Change PR83 to NC
EC-P-SIV-25	37		PU3	Change PU3 to RT8241E for VCCS voltage level
EC-P-SIV-26	38		PJP9	Change to default short
EC-P-SIV-27	39		PL8,PL9	Change PL8,PL9 footprint
EC-P-SIV-28	39		ER5,EC5	Add ER5,EC5 for EMI request
EC-P-SIV-29	39		PC20	Change PC20 to 0.22uF for CPU transient
EC-P-SIV-30	39		RV10	Add RV10 for ESD request
EC-P-SIV-31	39		PR23	Change PR23 to 20K for CPU IMON
EC-P-SIV-32	39		PR34	Change PR34 to 604ohm for GFX OCP&loadline



PROJECT: LZ7

Quanta Computer Inc.

Size	Document Number	Rev
	Power EC List	
Date:	Wednesday, December 21, 2011	Sheet 42 of 42